MC145574/D
REV 6

# MC145574

## ISDN S/T-Interface Transceiver



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# MC145574

## ISDN S/T-Interface Transceiver

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# MC145574 TABLE OF CONTENTS

# MC145574 ISDN S/T-INTERFACE TRANSCEIVER

## SECTION 1
### INTRODUCTION


| | | |
|---|---|---|
| 1.1 | INTRODUCTION | 1–1 |
| 1.2 | ORGANIZATION OF DATA SHEET | 1–1 |
| 1.3 | FEATURES | 1–2 |
| 1.4 | BLOCK DIAGRAM | 1–3 |
| 1.5 | PACKAGING | 1–3 |


## SECTION 2
### WIRING CONFIGURATIONS


| | | |
|---|---|---|
| 2.1 | INTRODUCTION | 2–1 |
| 2.2 | POINT–TO–POINT OPERATION | 2–1 |
| 2.3 | SHORT PASSIVE BUS OPERATION | 2–2 |
| 2.4 | EXTENDED PASSIVE BUS OPERATION | 2–2 |
| 2.5 | BRANCHED PASSIVE BUS OPERATION | 2–3 |
| 2.6 | NT1 STAR MODE OF OPERATION | 2–3 |


## SECTION 3
### ACTIVATION/DEACTIVATION OF S/T TRANSCEIVER


| | | |
|---|---|---|
| 3.1 | INTRODUCTION | 3–1 |
| 3.2 | TRANSMISSION STATES FOR NT MODE S/T TRANSCEIVER | 3–1 |
| 3.3 | TRANSMISSION STATES FOR TE MODE S/T TRANSCEIVER | 3–1 |
| 3.4 | ACTIVATION OF S/T LOOP BY NT | 3–1 |
| 3.5 | ACTIVATION OF S/T LOOP BY TE | 3–2 |
| 3.6 | ACTIVATION PROCEDURES IGNORED | 3–2 |
| 3.7 | FRAME SYNC | 3–2 |
| 3.7.1 | NT Mode | 3–2 |
| 3.7.2 | TE Mode | 3–2 |
| 3.8 | ACTIVATION INDICATION | 3–2 |
| 3.9 | NR1(2) — ERROR INDICATION (EI) | 3–2 |
| 3.10 | DEACTIVATION PROCEDURES | 3–3 |
| 3.11 | INITIAL STATE OF B1 AND B2 CHANNELS | 3–3 |
| 3.11.1 | NT | 3–3 |
| 3.11.2 | TE | 3–3 |
| 3.12 | ADDITIONAL NOTES | 3–3 |
| 3.12.1 | M and N Parameters | 3–3 |
| 3.12.2 | Echo Channel | 3–3 |
| 3.12.3 | A Bit | 3–4 |
| 3.12.4 | SCP Nomenclature | 3–4 |
| 3.12.5 | SCP Indication of Transmit and Receive States | 3–4 |

# MC145574 TABLE OF CONTENTS

## SECTION 4
### THE INTERCHIP DIGITAL LINK


| | | |
|---|---|---|
| 4.1 | INTRODUCTION | 4–1 |
| 4.2 | SIGNAL DESCRIPTION | 4–1 |
| 4.3 | IDL2 STANDARD MODE | 4–2 |
| 4.3.1 | NT IDL2 Slave | 4–2 |
| 4.3.2 | NT IDL2 Master | 4–3 |
| 4.3.3 | TE IDL2 Master | 4–3 |
| 4.3.4 | TE IDL2 Master Free Run | 4–3 |
| 4.3.5 | TE IDL2 Slave | 4–3 |
| 4.3.6 | Additional Notes | 4–4 |
| 4.3.6.1 | Phase Relationship of the NT Transmit Signal with Respect to FSC/FSR | 4–4 |
| 4.3.6.2 | Phase Relationship of the TE Transmit Signal with Respect to FSC/FSR, When in the IDL2 Master Mode | 4–4 |
| 4.3.6.3 | Operation of Multiple MC145574s in TE Slave Mode | 4–4 |
| 4.3.6.4 | Independent Tx/Rx Frame Syncs | 4–4 |
| 4.3.6.5 | Timeslot Assignment | 4–4 |
| 4.3.6.6 | Short and Long Framing | 4–8 |
| 4.3.6.7 | $\overline{\text{TSEN}}$ Signal | 4–9 |
| 4.3.6.8 | Miscellaneous | 4–9 |
| 4.3.6.9 | IDL2 Waveform Diagrams | 4–9 |


## SECTION 5
### SERIAL CONTROL PORT


| | | |
|---|---|---|
| 5.1 | INTRODUCTION | 5–1 |
| 5.2 | SCP TRANSACTIONS | 5–1 |
| 5.2.1 | SCP Nibble Register Read | 5–1 |
| 5.2.2 | SCP Nibble Register Write | 5–2 |
| 5.2.3 | SCP Byte Register Read | 5–3 |
| 5.2.4 | SCP Byte Register Write | 5–4 |
| 5.2.5 | SCP Merged Read/Write | 5–5 |
| 5.3 | SIGNAL DESCRIPTION | 5–6 |
| 5.3.1 | SCP Tx | 5–6 |
| 5.3.2 | SCP Rx | 5–6 |
| 5.3.3 | $\overline{\text{SCPCLK}}$ | 5–6 |
| 5.3.4 | $\overline{\text{SCPEN}}$ | 5–7 |
| 5.3.5 | $\overline{\text{IRQ}}$ | 5–7 |
| 5.4 | SCP HIGH–IMPEDANCE DIGITAL OUTPUT MODE (SCP HIDOM) | 5–7 |
| 5.5 | ADDITIONAL NOTES | 5–7 |
| 5.5.1 | SCP Independent of Crystal | 5–7 |
| 5.5.2 | SCP Slave | 5–7 |


## SECTION 6
### GENERAL CIRCUIT INTERFACE


| | | |
|---|---|---|
| 6.1 | OVERVIEW | 6–1 |
| 6.2 | GCI FRAME STRUCTURE | 6–1 |
| 6.3 | ENABLING THE GCI MODES | 6–1 |
| 6.4 | GCI INDIRECT MODE | 6–4 |
| 6.5 | GCI DIRECT MODE | 6–6 |
| 6.5.1 | Slave Mode | 6–6 |

# MC145574 TABLE OF CONTENTS

## SECTION 6 (continued)


| | | |
|---|---|---|
| 6.5.2 | Master Mode | 6–6 |
| 6.6 | 2B+D CHANNELS | 6–7 |
| 6.7 | M AND A/E CHANNELS | 6–7 |
| 6.7.1 | Monitor Channel Operation | 6–8 |
| 6.8 | MONITOR CHANNEL MESSAGES | 6–8 |
| 6.8.1 | Monitor Channel Commands | 6–10 |
| 6.8.2 | Monitor Channel Response Messages | 6–10 |
| 6.8.3 | Monitor Channel Status Indication Messages | 6–10 |
| 6.8.4 | Accessible Monitor Channel Registers | 6–11 |
| 6.8.5 | SCP/GCI Register Differences | 6–12 |
| 6.9 | COMMAND INDICATE CHANNEL OPERATION | 6–12 |
| 6.10 | GCI ACTIVATION AND DEACTIVATION TIMING DIAGRAMS | 6–14 |


## SECTION 7
### PIN DESCRIPTIONS


| | | |
|---|---|---|
| 7.1 | INTRODUCTION | 7–1 |
| 7.2 | PIN DESCRIPTIONS | 7–1 |
| 7.2.1 | ISET | 7–1 |
| 7.2.2 | RxN, RxP | 7–1 |
| 7.2.3 | TE/$\overline{\text{NT}}$ | 7–2 |
| 7.2.4 | M/$\overline{\text{S}}$ | 7–2 |
| 7.2.5 | T_IN/TFSC/TCLK/FIX | 7–2 |
| 7.2.6 | $V_{SS}$ | 7–2 |
| 7.2.7 | SG/DGRANT/ANDOUT | 7–2 |
| 7.2.8 | DREQUEST/ANDIN | 7–2 |
| 7.2.9 | CLASS/ECHO_IN | 7–3 |
| 7.2.10 | FSC/FSR | 7–3 |
| 7.2.11 | DCL | 7–3 |
| 7.2.12 | $D_{in}$ | 7–3 |
| 7.2.13 | $D_{out}$ | 7–3 |
| 7.2.14 | SCP Tx/S0/M0 | 7–3 |
| 7.2.15 | SCP Rx/S1/M1 | 7–3 |
| 7.2.16 | $\overline{\text{SCPCLK}}$/S2/M2 | 7–3 |
| 7.2.17 | $\overline{\text{SCPEN}}$/$\overline{\text{GCIEN}}$ | 7–3 |
| 7.2.18 | $\overline{\text{TSEN}}$/FST/BCL/LBA | 7–3 |
| 7.2.19 | $\overline{\text{IRQ}}$/$\overline{\text{IND}}$ | 7–4 |
| 7.2.20 | $V_{DD}3$ | 7–4 |
| 7.2.21 | $V_{DD}$ I/O | 7–4 |
| 7.2.22 | $V_{DD}5$ | 7–4 |
| 7.2.23 | EXTAL | 7–4 |
| 7.2.24 | XTAL | 7–4 |
| 7.2.25 | TxN, TxP | 7–4 |
| 7.2.26 | $\overline{\text{RESET}}$ | 7–4 |
| 7.3 | ADDITIONAL NOTES | 7–5 |
| 7.3.1 | Input Levels | 7–5 |
| 7.3.2 | Output Levels | 7–5 |
| 7.3.3 | SCP HIDOM | 7–5 |

# MC145574 TABLE OF CONTENTS

## SECTION 8
### NIBBLE REGISTER MAP DEFINITION


8.1 INTRODUCTION . . . . . 8–1
8.2 NR0 . . . . . 8–2
8.3 NR1 . . . . . 8–3
8.4 NR2 . . . . . 8–3
8.5 NR3 . . . . . 8–4
8.6 NR4 . . . . . 8–5
8.7 NR5 . . . . . 8–6
8.8 NR6 . . . . . 8–7
8.9 NR7 . . . . . 8–8


## SECTION 9
### BYTE REGISTER MAP DEFINITION


9.1 INTRODUCTION . . . . . 9–1
9.2 BR0 . . . . . 9–3
9.3 BR1 . . . . . 9–3
9.4 BR2 . . . . . 9–3
9.5 BR3 . . . . . 9–3
9.6 BR4 . . . . . 9–4
9.7 BR5 . . . . . 9–5
9.8 BR6 . . . . . 9–5
9.9 BR7 . . . . . 9–6
9.10 BR8 . . . . . 9–8
9.11 BR9 . . . . . 9–8
9.12 BR10 . . . . . 9–9
9.13 BR11 . . . . . 9–10
9.14 BR12 . . . . . 9–12
9.15 BR13 . . . . . 9–12
9.16 BR14 . . . . . 9–13
9.17 BR15 . . . . . 9–13


## SECTION 10
### OVERLAY REGISTER MAP DEFINITION


10.1 INTRODUCTION . . . . . 10–1
10.2 OR0 . . . . . 10–2
10.3 OR1 . . . . . 10–2
10.4 OR2 . . . . . 10–2
10.5 OR3 . . . . . 10–3
10.6 OR4 . . . . . 10–3
10.7 OR5 . . . . . 10–3
10.8 OR6 . . . . . 10–4
10.9 OR7 . . . . . 10–5
10.10 OR8 . . . . . 10–6
10.11 OR9 . . . . . 10–7
10.12 OR15 . . . . . 10–7

# MC145574 TABLE OF CONTENTS

## SECTION 11
### D CHANNEL OPERATION


| | | |
|---|---|---|
| 11.1 | INTRODUCTION | 11–1 |
| 11.2 | IDL2 D CHANNEL OPERATION | 11–2 |
| 11.2.1 | Gaining Access to the D Channel in the TE Mode | 11–2 |
| 11.2.2 | Setting the Class for TE Mode of Operation | 11–2 |
| 11.2.3 | Generation of an Interrupt in the TE Mode | 11–3 |
| 11.2.4 | Gaining Access to the D Channel in the NT Mode | 11–3 |
| 11.2.5 | GCI D Channel Operation | 11–3 |


## SECTION 12
### MULTIFRAMING


| | | |
|---|---|---|
| 12.1 | INTRODUCTION | 12–1 |
| 12.2 | ACTIVATION/DETECTION OF MULTIFRAMING IN THE MC145574 | 12–1 |
| 12.3 | WRITING S CHANNEL DATA TO AN NT–CONFIGURED MC145574 | 12–1 |
| 12.4 | MULTIFRAME INTERRUPTS IN AN NT–CONFIGURED MC145574 | 12–2 |
| 12.5 | READING Q CHANNEL DATA FROM AN NT–CONFIGURED MC145574 | 12–3 |
| 12.6 | WRITING Q CHANNEL DATA TO A TE–CONFIGURED MC145574 | 12–3 |
| 12.7 | MULTIFRAME INTERRUPTS IN A TE–CONFIGURED MC145574 | 12–3 |
| 12.8 | READING S SUBCHANNEL DATA FROM A TE–CONFIGURED MC145574 | 12–3 |
| 12.9 | MULTIFRAMING IN GCI MODE | 12–3 |


## SECTION 13
### DEVICE CONFIGURATIONS


| | | |
|---|---|---|
| 13.1 | NT CONFIGURATIONS | 13–1 |
| 13.1.1 | NT Fixed or Adaptive Timing | 13–1 |
| 13.1.2 | NT Master or Slave | 13–1 |
| 13.1.3 | NT1 Star and NT Terminal Modes | 13–2 |
| 13.1.3.1 | NT1 Star Mode | 13–2 |
| 13.1.3.2 | NT Terminal Mode | 13–4 |
| 13.2 | TE CONFIGURATIONS | 13–4 |
| 13.2.1 | TE Master Mode (TEM) | 13–5 |
| 13.2.2 | TE Slave Mode (TES) | 13–5 |


## SECTION 14
### CLOCK INTERFACE

## SECTION 15
### INTERRUPTS


| | | | |
|---|---|---|---|
| 15.1 | INTRODUCTION | | 15–1 |
| 15.2 | IRQ7 | NR3(0) — NT : D CHANNEL COLLISION<br>TE : NOT APPLICABLE | |
| | | NR4(0) — ENABLE | 15–1 |
| 15.3 | IRQ1 | NR3(1) — TE: D CHANNEL COLLISION<br>NT: NOT APPLICABLE | |
| | | NR4(1) — ENABLE | 15–1 |
| 15.4 | IRQ2 | NR3(2) — MULTIFRAME RECEPTION | |
| | | NR4(2) — ENABLE | 15–1 |

# MC145574 TABLE OF CONTENTS

## SECTION 15 (continued)


15.5 IRQ3 NR3(3) — CHANGE IN Rx INFO STATE
NR4(3) — ENABLE . . . . . 15–2
15.6 IRQ6 NR3(1) — NT: FAR–END CODE VIOLATION (FECV) DETECTION
TE: NOT APPLICABLE
NR4(1) — ENABLE . . . . . 15–2
15.7 GCI MODE . . . . . 15–2


## SECTION 16
### TRANSMISSION LINE INTERFACE CIRCUITRY


16.1 INTRODUCTION . . . . . 16–1
16.2 TRANSMIT LINE INTERFACE CIRCUITRY . . . . . 16–1
16.3 RECEIVE LINE INTERFACE CIRCUITRY . . . . . 16–1
16.4 ADDITIONAL NOTES . . . . . 16–3
16.4.1 Sources of Line Interface Transformers . . . . . 16–3
16.4.2 Termination Resistors . . . . . 16–3
16.4.3 Protection Diodes . . . . . 16–3


## SECTION 17
### POWER MODE OPERATION


17.1 POWER SUPPLY STRATEGY . . . . . 17–1
17.2 POWER MODES . . . . . 17–1
17.2.1 Normal Operation . . . . . 17–1
17.2.2 Transmit Power–Down . . . . . 17–1
17.2.3 Absolute Minimum Power . . . . . 17–2
17.2.4 Sleep . . . . . 17–2


## SECTION 18
### ELECTRICAL SPECIFICATIONS


18.1 MAXIMUM RATINGS . . . . . 18–1
18.2 DIGITAL DC ELECTRICAL CHARACTERISTICS . . . . . 18–1
18.3 ANALOG CHARACTERISTICS . . . . . 18–2
18.4 POWER DISSIPATION . . . . . 18–2
18.5 IDL2 TIMING CHARACTERISTICS . . . . . 18–3
18.5.1 IDL2 Master Timing, 8– and 10–Bit Formats . . . . . 18–3
18.5.2 IDL2 Slave Timing, 8– and 10–Bit Formats . . . . . 18–4
18.6 GCI TIMING FOR MASTER AND SLAVE MODE . . . . . 18–6
18.7 SCP TIMING CHARACTERISTICS . . . . . 18–8
18.8 NT1 STAR MODE TIMING CHARACTERISTICS . . . . . 18–9
18.9 D CHANNEL TIMING CHARACTERISTICS (IDL2 MODE) . . . . . 18–9

# MC145574 TABLE OF CONTENTS

## SECTION 19
### MECHANICAL DATA


| | | |
|---|---|---|
| 19.1 | PIN ASSIGNMENTS | 19–1 |
| 19.2 | PACKAGE DIMENSIONS | 19–2 |


## SECTION 20
### F57J4 MASK SET DIFFERENCES


| | | |
|---|---|---|
| 20.1 | FUNCTIONAL DIFFERENCES | 20–1 |
| 20.1.1 | Differences in Section 6 | 20–1 |
| 20.1.2 | Differences in Section 10 | 20–1 |
| 20.1.3 | Differences in Section 13.1.3.2 | 20–1 |


## APPENDIX A
### MC145574EVK ISDN S/T–INTERFACE TRANSCEIVER EVALUATION KIT


| | | |
|---|---|---|
| A.1 | INTRODUCTION | A–1 |
| A.2 | FEATURES | A–2 |
| A.2.1 | General | A–2 |
| A.2.2 | Hardware | A–2 |
| A.2.3 | Software | A–2 |
| A.3 | BLOCK DIAGRAM | A–3 |


## APPENDIX B
### GLOSSARY OF TERMS AND ABBREVIATIONS

# MC145574 LIST OF FIGURES


| | | |
|---|---|---|
| Figure 1–1. | Block Diagram | 1–3 |
| Figure 2–1. | Point–to–Point | 2–1 |
| Figure 2–2. | Short Passive Bus | 2–2 |
| Figure 2–3. | Extended Passive Bus | 2–2 |
| Figure 2–4. | Branched Passive Bus | 2–3 |
| Figure 4–1. | Phase Relationship of NT Transmit Signal | 4–5 |
| Figure 4–2. | Two–Baud Turnaround in TE | 4–6 |
| Figure 4–3. | Phase Relationship of TE Transmit Signal | 4–7 |
| Figure 4–4. | Example Architecture of an NT2 | 4–8 |
| Figure 4–5. | Standard IDL2 10–Bit Mode | 4–10 |
| Figure 4–6. | Standard IDL2 8–Bit Mode with Long Frame Sync | 4–10 |
| Figure 4–7. | Standard IDL2 8–Bit Slave Mode with Independent Frame Syncs | 4–10 |
| Figure 4–8. | Timeslot Operation with Independent Slave Frame Syncs, TSEN | 4–11 |
| Figure 5–1. | Serial Control Port Nibble Register Read Operation | 5–2 |
| Figure 5–2. | Serial Control Port Nibble Register Write Operation | 5–2 |
| Figure 5–3. | Serial Control Port Byte Register Read Operation | 5–3 |
| Figure 5–4. | Serial Control Port Byte Register Read Operation Double 8–Bit Transaction | 5–4 |
| Figure 5–5. | Serial Control Port Byte Register Write Operation | 5–4 |
| Figure 5–6. | Serial Control Byte Register Write Operation Double 8–Bit Transaction | 5–5 |
| Figure 5–7. | Merged Serial Control Port Nibble Register Read Operation | 5–5 |
| Figure 6–1. a. | Relative Channel Positions (GCI Slave Mode) | 6–2 |
| Figure 6–1. b. | Relative Channel Positions (GCI Master Mode) | 6–3 |
| Figure 6–2. | GCI Indirect Mode | 6–4 |
| Figure 6–3. | Monitor Channel Access Protocol | 6–9 |
| Figure 6–4. | Activation from TE End | 6–14 |
| Figure 6–5. | Deactivation from NT End | 6–15 |
| Figure 6–6. | Activation from NT End | 6–15 |
| Figure 7–1. | Pin Assignments | 7–1 |
| Figure 11–1. | SCIT Terminal Mode | 11–4 |
| Figure 13–1. | NT Family Tree | 13–1 |
| Figure 13–2. | NT1 Star Mode of Operation | 13–3 |
| Figure 13–3. | NT2 Architecture | 13–6 |
| Figure 14–1. | Typical Crystal Oscillator Connection | 14–1 |
| Figure 14–2. | Connection with External Clock | 14–1 |
| Figure 16–1. | Transmit Line Interface Circuit | 16–2 |
| Figure 16–2. | Receive Line Interface Circuit | 16–2 |
| Figure 18–1. | IDL2 Master Timing, 8– and 10–Bit Formats | 18–3 |
| Figure 18–2. | IDL2 Slave Timing, 8– and 10–Bit Formats | 18–5 |
| Figure 18–3. | GCI Timing For Master and Slave Mode | 18–7 |
| Figure 18–4. | SCP Timing Characteristics | 18–8 |
| Figure 18–5. | NT1 Star Mode | 18–9 |
| Figure 18–6. | D Channel Request Timing | 18–9 |
| Figure 18–7. | D Channel Grant Timing | 18–9 |
| Figure 19–1. | MC145574DW Pin Assignment (SOIC 28–Pin Package, Case 751F) | 19–1 |
| Figure 19–2. | MC145574PB Pin Assignment (TQFP 32–Pin Package, Case 873A) | 19–1 |
| Figure A–1. | Motorola Silicon Applications and the MC145574EVK | A–1 |
| Figure A–2. | Block Diagram | A–3 |

# MC145574 LIST OF TABLES


| | | |
|---|---|---|
| Table 3–1. | NT Mode Transmission States | 3–1 |
| Table 3–2. | TE Mode Transmission States | 3–1 |
| Table 4–1. | IDL2 Clock Speeds | 4–2 |
| Table 6–1. | CLK1, CLK0 GCI Clock Selection | 6–4 |
| Table 6–2. | GCI Timeslot Assignment | 6–5 |
| Table 6–3. | M2, M1, and M0 Pins in GCI NT Master Mode | 6–6 |
| Table 6–4. | M2, M1, and M0 Pins in GCI TE Master Mode | 6–7 |
| Table 6–5. | Monitor Channel Commands | 6–10 |
| Table 6–6. | Monitor Channel Response Messages | 6–10 |
| Table 6–7. | Monitor Channel Status Indication Messages | 6–10 |
| Table 6–8. | C/I Channel Commands and Indications | 6–13 |
| Table 6–9. | GCI C/I Codes | 6–13 |
| Table 8–1. | SCP Nibble Register Map for NT Operation | 8–1 |
| Table 8–2. | SCP Nibble Register Map for TE Operation | 8–1 |
| Table 8–3. | Nibble Register Initialization After Any Reset | 8–2 |
| Table 9–1. | Byte Register Map for NT Mode of Operation | 9–1 |
| Table 9–2. | Byte Register Map for TE Mode of Operation | 9–2 |
| Table 9–3. | Byte Register Initialization After Any Reset | 9–2 |
| Table 9–4. | IDL2 Clock Speed Codes | 9–8 |
| Table 9–5. | BR11(5), BR11(4) Rx INFO State Codes | 9–11 |
| Table 9–6. | BR11(3), BR11(2) Tx INFO State Codes | 9–11 |
| Table 10–1. | Overlay Register Map | 10–1 |
| Table 10–2. | Overlay Register Initialization After Any Reset | 10–2 |
| Table 10–3. | S(2:0) GCI Timeslot Assignment | 10–3 |
| Table 10–4. | S(2:0) GCI Timeslot Assignment | 10–4 |
| Table 11–1. | Channel SCP Bit Description | 11–1 |
| Table 11–2. | D Channel Operation Pin Description | 11–1 |
| Table 11–3. | MC145574 Class Operations | 11–2 |
| Table 12–1. | S Channel Data Transmission | 12–2 |
| Table 12–2. | Multiframe Interrupts | 12–2 |
| Table 12–3. | TE Multiframe Interrupts | 12–3 |
| Table 13–1. | Pin Operations | 13–2 |
| Table 13–2. | Pin Operations for Master and Slave Modes | 13–4 |

# 1
# INTRODUCTION

## 1.1 INTRODUCTION

The MC145574 is Motorola's second generation S/T transceiver and is a follow–up to the MC145474/75 transceiver.

The MC145574 provides the improved interfacing capabilities and reduced power consumption required by today's ISDN applications, while maintaining the functionality and extended range performance of the MC145474/75.

The MC145574 provides an economical VLSI layer 1 interface for the transportation of two 64 kbps B channels and one 16 kbps D channel between the network termination (NT) and terminal equipment applications (TEs). The MC145574 conforms to CCITT I.430, ETSI ETS 300012, and ANSI T1.605 specifications.

The MC145574 provides the modulation/line drive and demodulation/line receive functions required of the interface. In addition, the MC145574 provides the activation/deactivation, error monitoring, framing, bit, and octet timing. The MC145574 provides the control signals for the interface to the layer 2 devices. Complete multiframe capability is provided.

The MC145574 features the interchip digital link (IDL2) for the exchange of the 2B+D channel information between ISDN components and systems. The MC145574 provides an industry standard serial control port (SCP) to program the operation of the transceiver. As an alternative to the IDL2+SCP combination, a general circuit interface (GCI) is provided.

The MC145574 is not pin compatible with the MC145474/75, but it does have a compatible register set. However, to make full use of the additional MC145574 features, software enhancements are required.

## 1.2 ORGANIZATION OF DATA SHEET

This data sheet is comprised of 20 sections. Section 1 is an introduction, serving to outline the features, package types, and pin assignments of the MC145574. Section 2 describes the various wiring configurations which are applicable to the MC145574, and the operational distances as recommended by CCITT I.430, ETSI ETS 300012, and ANSI T1.605. Section 3 addresses the activation and deactivation procedures of the MC145574.

The MC145574 incorporates the IDL2. This is a four–wire interface used for full–duplex communication between ICs on the board level. Two 64 kbps B channels and one 16 kbps D channel are transmitted and received over this interface. Section 4 is a detailed description of the IDL2.

The MC145574 incorporates an SCP interface. The SCP is a four–wire interface conforming to an industry standard multi–drop serial link. The SCP is compatible with Motorola's serial peripheral interface (SPI). The SCP makes use of seven nibble registers, 16 byte registers and 10 overlay registers. Section 5 is a description of the SCP. A per bit description of the nibble, byte, and overlay registers is provided in Sections 8, 9, and 10, respectively. When the MC145574 is configured as a TE, it is equipped with five interrupt modes. When configured as an NT, it is equipped with four interrupt modes. Section 15 describes these interrupts.

The MC145574 also features a GCI interface. This is a standard four–wire interface which allows full–duplex transmission of two 64 kbps B channels and one 16 kbps D channel, multiplexed with control and maintenance information channels. Section 6 is a description of the GCI.

Section 7 contains pin descriptions of the MC145574. The pin descriptions differentiate between the device configured for NT mode or TE mode of operation, and GCI and IDL2+SCP.

As mentioned previously, the MC145574 is used for the transmission of two 64 kbps B channels and one 16 kbps D channel. Access to the B channels is determined by the network. The TEs gain access to the D channel in accordance with CCITT I.430, ETSI ETS 300012, and ANSI T1.605 recommendations. A description of the D channel operation is contained in Section 11.

In addition to the 2B+D channels, the S/T transceiver has a multiframing capability. Multiframing is a layer 1 signalling channel for use between the NT and the TE(s). The multiframing operation is described in Section 12.

The MC145574 can be configured in several different operating modes depending on the application. Section 13 describes all the possible configurations, whether in the NT or TE mode.

Section 16 describes how to interface the MC145574 to the S/T bus. Section 17 describes the various power modes of operation. Section 18 contains electrical specifications, and Section 19 contains mechanical data relevant to the MC145574. Section 20 describes the differences between this data book and the F57J4 mask version of the MC145574.

## 1.3 FEATURES

The features of the MC145574 are described below.

- Conforms to CCITT I.430, ETSI ETS 300012, and ANSI T1.605 Specifications
- Register Compatible With the First Generation MC145474/75
- Exceeds Q.502 Jitter Requirements for TE Slave Applications
- Pin Selectable NT or TE Modes of Operation
- Incorporates the IDL2, With Timeslot Assigner
- Industry Standard Microprocessor SCP
- GCI Interface
- Uses 2.5:1 Transformers for Transmit and Receive
- Exceeds the Recommended Range of Operation in All Configurations
- Complete Multiframing Capability Supported (SC1 – SC5 and Q Channel)
- Optional B Channel Idle, Invert, or Exchange
- Supports Full Range of S/T and IDL2 Loopbacks
- Supports Transmit Power–Down, Listening, and Absolute Minimum Power Modes
- Supports Crystal or External Clock Input Mode
- NT Star and NT Terminal Modes Supported
- Low Power Consumption
- Compatible with 3 V Devices

## 1.4 BLOCK DIAGRAM

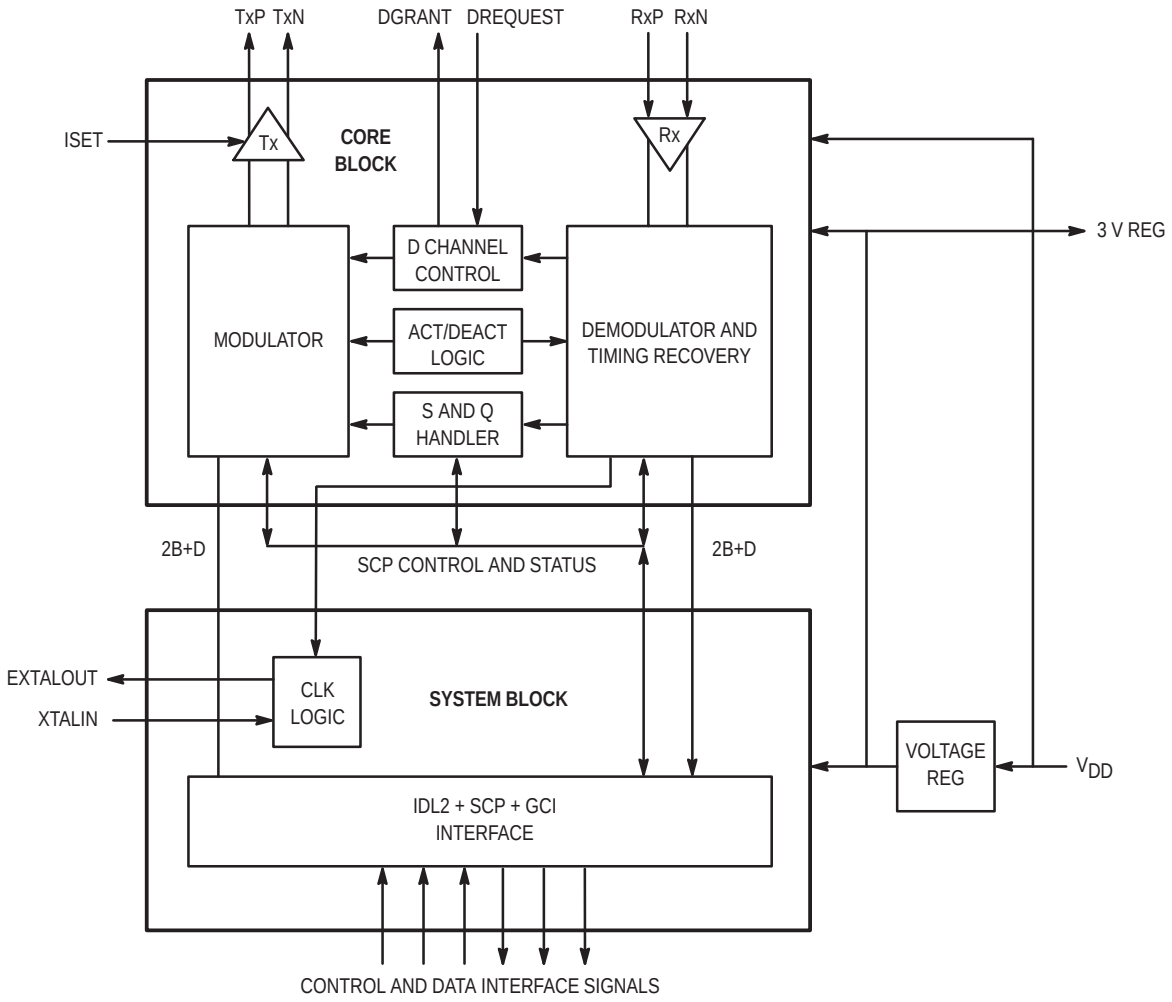



**Figure 1–1. Block Diagram**

## 1.5 PACKAGING

The MC145574 comes in the following packages:

28–Pin, 600 mil Wide, Plastic SOIC
32–Pin, 700 mil Square, TQFP

The pin assignments for the MC145574 are described in Section 7. Package dimensions are in Section 19.

# 2
# WIRING CONFIGURATIONS

## 2.1 INTRODUCTION

The MC145574 ISDN S/T transceiver conforms to CCITT I.430, ETSI ETS 300012, and ANSI T1.605 specifications. It is a layer 1 transceiver designed for use at the ISDN S and T reference points. It is designed for both point–to–point and multipoint operation. The S/T transceiver is designed for use in either the network terminating (NT) mode or in the terminal endpoint (TE) applications. Two 64 kpbs B channels and one 16 kbps D channel are transmitted in a full–duplex fashion across the interface.

Sections 2.2 through 2.6 contain suggested wiring configurations for use. These configurations are deemed to be the most common but by no means the only wiring configurations. Section 16 specifies the recommended circuitry for interfacing the MC145574 to the S/T bus. Note that when operating in the TE mode, only one TE has the 100 Ω termination resistors in the transmit and receive paths. Figures 2–1 through 2–4 illustrate where to connect the termination resistors for the described loop configurations.

A description of the most commonly used loop configurations is as described below.

## 2.2 POINT-TO-POINT OPERATION

In the point–to–point mode of operation, one NT communicates with one TE. As such, 100 Ω termination resistors must be connected across the transmit and receive paths of both the NT and TE transceivers. Figure 2–1 illustrates this wiring configuration.

When using the MC145574 in this configuration, the NT must be in adaptive timing. This is accomplished by holding the FIX pin low; i.e., connecting it to $V_{SS}$. Refer to Section 6 for a more detailed description of this pin function. CCITT I.430, ETSI ETS 300012, and ANSI T1.605 specify that the S/T transceiver must be able to operate up to a distance of 1 km in the point–to–point mode. This is the distance D1 as shown in Figure 2–1.

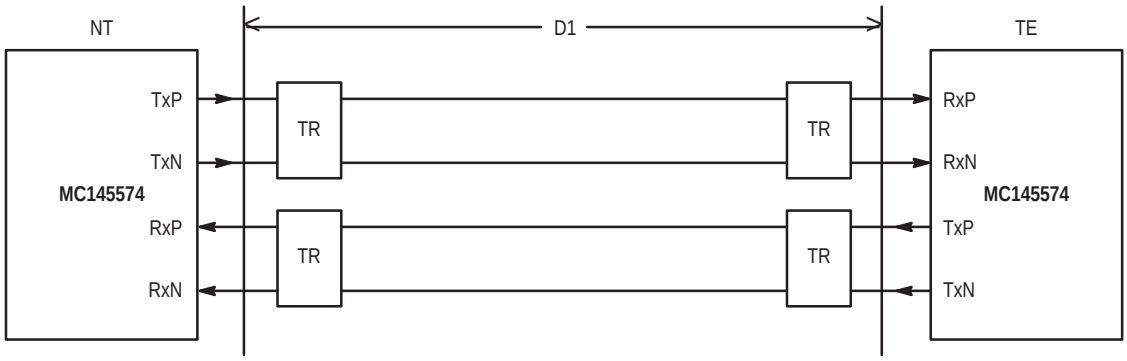



**Figure 2–1. Point–to–Point**

## 2.3 SHORT PASSIVE BUS OPERATION

The short passive bus is intended for use when up to eight TEs are required to communicate with one NT. The TEs can be distributed at any point along the passive bus, the only requirement being that the termination resistors be located at the end of the passive bus. Figure 2–2 illustrates this wiring configuration. CCITT I.430, ETSI ETS 300012, and ANSI T1.605 specify a maximum operational distance from the NT of 200 meters. This corresponds to the distance D2 as shown in Figure 2–2.

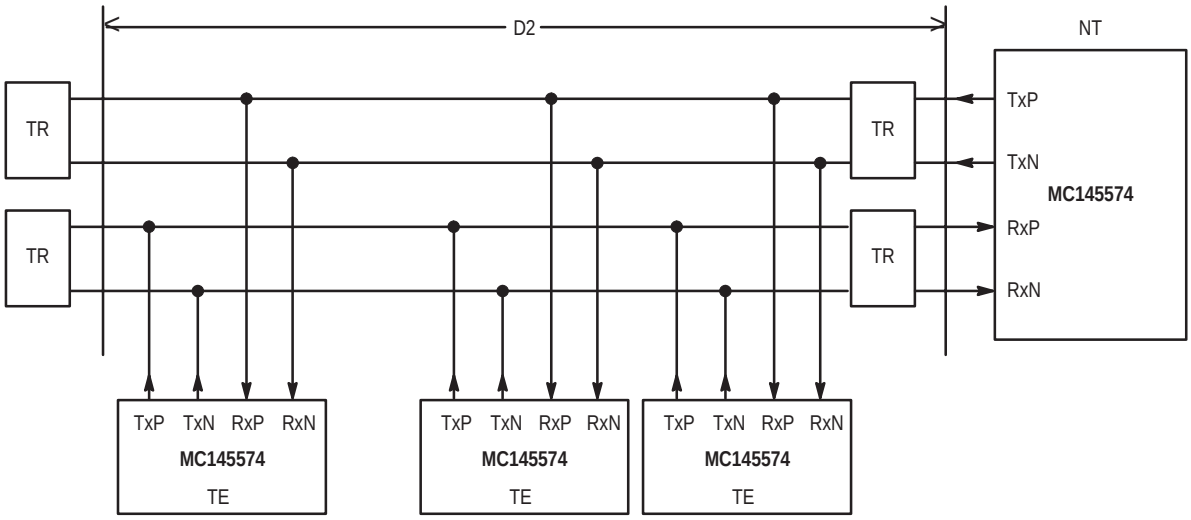



**Figure 2–2. Short Passive Bus**

## 2.4 EXTENDED PASSIVE BUS OPERATION

A wiring configuration whereby the TEs are restricted to a grouping at the far end of the cable, distant from the NT, is shown as the “Extended Passive Bus.” This configuration is shown in Figure 2–3. The termination resistors are to be positioned as shown in Figure 2–3.

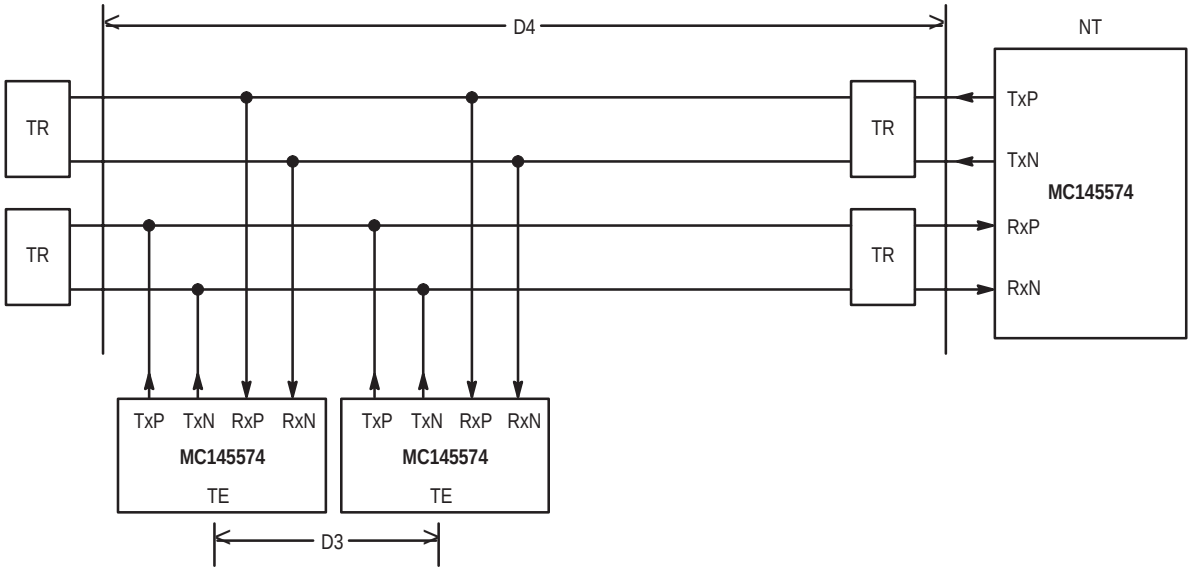



**Figure 2–3. Extended Passive Bus**

The essence of this configuration is that a restriction is placed on the distance between the TEs. The distance, D3 (as shown in Figure 2–3), corresponds to the maximum distance between the grouping of TEs. CCITT I.430, ETSI ETS 300012, and ANSI T1.605 specify a distance of 25 – 50 meters for the separation between the TEs, and a distance of 500 meters for the total length. These distances correspond to the distances D3 and D4 as shown in Figure 2–3.

Note that the “NT configured” MC145574 should be placed in the adaptive timing mode for this configuration. This is achieved by holding the FIX pin low.

## 2.5 BRANCHED PASSIVE BUS OPERATION

A wiring configuration which has somewhat similar characteristics to those of the “extended passive bus” is known as the “branched passive bus” and is shown in Figure 2–4. In this configuration the branching occurs at the end of the bus. The branching occurs after a distance D1 from the NT. The distance D5 corresponds to the maximum separation between the TEs.

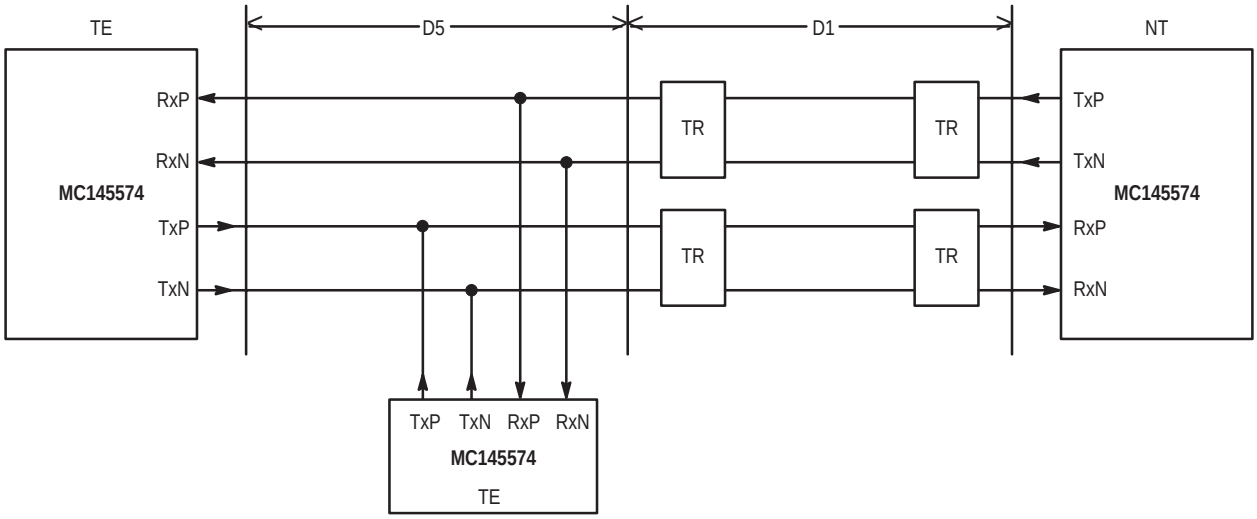



**Figure 2–4. Branched Passive Bus**

## 2.6 NT1 STAR MODE OF OPERATION

A wiring configuration which may be used to support multiple T interfaces is known as the “NT1 Star mode of operation.” This mode of operation is supported by the MC145574. This mode is described in Section 11. Note that the NT1 Star mode contains multiple NTs. Each of these NTs can be connected to either a passive bus (short, extended, or branched) or to a single TE.

# 3
# ACTIVATION/DEACTIVATION OF S/T TRANSCEIVER

## 3.1 INTRODUCTION

CCITT I.430, ETSI ETS 300012, and ANSI T1.605 define five information states for the S/T transceiver. When the NT is in the fully operational state, it transmits INFO 4. When the TE is in the fully operational state, it transmits INFO 3. INFO 1 is transmitted by the TE when it wants to wake up the NT. INFO 2 is transmitted by the NT when it wants to wake up the TE, or in response to the TE's transmitted INFO 1. These states cause unique patterns of symbols to be transmitted over the S/T–interface. Only when the S/T loop is in the fully activated state are the 2B+D channels of data transmitted over the interface.

## 3.2 TRANSMISSION STATES FOR NT MODE S/T TRANSCEIVER

When configured as an NT, an S/T transceiver can be in any of the following transmission states shown in Table 3–1.

**Table 3–1. NT Mode Transmission States**

| Information State | Description |
|---|---|
| INFO 0 | The NT transmits 1s in every bit position. This corresponds to no signal being transmitted. |
| INFO 2 | The NT sets its B1, B2, D, and E channels to 0. The A bit is set to 0. (See Sections 3.12.1 and 3.12.2.) |
| INFO 4 | INFO 4 corresponds to frames containing operational data on the B1, B2, D, and E channels. The A bit is set to 1. |

## 3.3 TRANSMISSION STATES FOR TE MODE S/T TRANSCEIVER

When configured as a TE, an S/T transceiver can be in any of the following transmission states shown in Table 3–2.

**Table 3–2. TE Mode Transmission States**

| Information State | Description |
|---|---|
| INFO 0 | The TE transmits 1s in every bit position. This corresponds to no signal being transmitted. |
| INFO 1 | The TE transmits a continuous signal with the following pattern: positive 0, negative 0, six 1s. This signal is asynchronous to the NT. |
| INFO 3 | INFO 3 corresponds to frames containing operational data on the B1, B2, and D channels. If INFO 4 or INFO 2 is being received, INFO 3 will be synchronized to it. |

## 3.4 ACTIVATION OF S/T LOOP BY NT

The NT activates the loop by transmitting INFO 2 to the TE(s). This is accomplished in the MC145574 by setting NR2(3) to a 1 (see Section 3.12.3). Note that this bit is internally reset to 0 after the internal activation state machine has recognized its active transition.

The TE on receiving INFO 2 synchronizes to it and transmits back INFO 3 to the NT. The NT, on receiving INFO 3 from the TE, responds with INFO 4, thus activating the loop.

## 3.5 ACTIVATION OF S/T LOOP BY TE

The TE activates an inactive loop by transmitting INFO 1 to the NT. This is accomplished in the MC145574 by setting NR2(3) to a 1. Note that this bit is internally reset to 0 after the internal activation state machine has recognized its active transition.

The NT, upon detecting INFO 1 from the TE, responds with INFO 2. The TE, upon receiving a signal from the NT, ceases transmission of INFO 1, reverting to transmitting INFO 0. After synchronizing to the received signal and having fully verified that it is INFO 2, the TE responds with INFO 3, thus activating the loop.

## 3.6 ACTIVATION PROCEDURES IGNORED

The MC145574 has the capability of being forced into the highest transmission state. This is accomplished by setting BR7(7) to a 1. Thus when this bit is set in the NT, it forces the NT to transmit INFO 4. Correspondingly, in the TE, setting this bit to 1 forces the TE to transmit INFO 3.

Note that CCITT I.430, ETSI ETS 300012, and ANSI T1.605 specifications allow a TE to be activated by reception of INFO 4, without having to go through the intermediate handshaking. This is to allow for the situation where a TE is connected to an already active loop.

However, an NT can not be activated by a TE sending it INFO 3, without going through the intermediate INFO 1, INFO 2, INFO 3, and INFO 4 states.

This “Activation Procedures Ignored” feature is provided for test purposes, allowing the NT to forcibly activate the TE(s). In the TE, the forced transmission of INFO 3 enables verification of the TEs operation.

## 3.7 FRAME SYNC

### 3.7.1 NT Mode

When the S/T transceiver in the NT mode is receiving INFO 3 from the TE(s) and has achieved frame synchronization, it sets the FSYNC status bit NR1(0) high.

### 3.7.2 TE Mode

When the TE is receiving either INFO 2 or INFO 4 from the NT, and has achieved frame synchronization, the MC145574 internally sets the SCP nibble bit, NR1(0). NR1(0) performs this function in both the NT and TE modes, for the MC145574.

## 3.8 ACTIVATION INDICATION

NR1(3), the activation indication bit, is used to signify that the loop is fully active. When the MC145574 is configured as an NT, this corresponds to the NT transmitting INFO 4 and receiving INFO 3. When the MC145574 is configured as a TE, this corresponds to it transmitting INFO 3 and receiving INFO 4. When the loop is in the fully active state, NR1(3) is internally set high.

## 3.9 NR1(2) — ERROR INDICATION (EI)

NR1(2) is set by the MC145574 S/T transceiver to indicate an error condition has been detected by the activation state machine of the transceiver, as outlined in CCITT I.430, ETSI ETS 300012, and ANSI T1.605. The low–to–high level transition of the EI bit corresponds to the EI1 error indication reporting, while the high–to–low level transition of the EI bit corresponds to the EI2 error indication reporting recovery. Note that NR1(2) is a read only bit.

## 3.10 DEACTIVATION PROCEDURES

CCITT I.430, ETSI ETS 300012, and ANSI T1.605 specifications dictate that only an NT can deactivate the S/T loop. Intuitively, this has to be the case because in a passive bus if one TE sends INFO 0, seeking to deactivate the loop, the other TE's INFO 3 simply overrides it.

An NT transmits INFO 0 to the TE(s) when it wishes to deactivate the S/T loop. This is done by setting NR2(2) (Deactivation Request) to a 1. Note that this bit is internally reset to 0 after the internal activation state machine has recognized its active transition.

## 3.11 INITIAL STATE OF B1 AND B2 CHANNELS

### 3.11.1 NT

When the MC145574 is configured as an NT, NR5(3:2) corresponds to "IDLE B1 channel on S/T loop", and "IDLE B2 channel on S/T loop", respectively. The device comes out of a hardware or software reset with these two bits reset to 0. Thus, the NT comes out of reset with the B1 and B2 channels enabled. When the NT is transmitting INFO 4, data on the B1 and B2 IDL2 timeslots will be modulated onto the S/T loop. Setting either of these nibble bits in the NT mode will idle the corresponding B channel on the S/T loop. Note that putting a B channel in the idle mode affects only the transmitted B channel. The demodulated B data is still transmitted out on IDL2 Tx, in accordance with the IDL2 specification.

### 3.11.2 TE

When the MC145574 is configured as a TE, NR5(3:2) corresponds to "ENABLE B1 channel on S/T loop," and "ENABLE B2 channel on S/T loop," respectively. The device comes out of a hardware or software reset with these two bits reset to 0. Thus, the TE comes out of reset with the B1 and B2 channels disabled. When the TE is transmitting INFO 3, data on the B1 and B2 IDL2 timeslots is not modulated onto the S/T loop. Setting either of these bits enables the modulation of the corresponding B channel onto the S/T loop.

Note that although the TE comes out of reset with both B channels in the idle mode, this only affects the modulation path. Demodulated data is still transmitted on $D_{out}$.

## 3.12 ADDITIONAL NOTES

### 3.12.1 M and N Parameters

For conformance qualification procedures, it is often necessary to state the values of M and N, where:

M is the number of successive good S0 frames for frame synchronization, and
N is the number of successive bad S0 frames for frame loss.

For the MC145574, M = 5 and N = 3.

### 3.12.2 Echo Channel

The NT demodulates the 2B+D data received from the TE(s). In addition to passing this data onto the network, the NT echoes the D channel data back to the TE(s) using the echo channel. This echo channel is monitored by the TEs and used in the D channel contention algorithm. For a detailed description, refer to Section 11.

### 3.12.3 A Bit

An S/T frame consists of 48 bauds. In the NT to TE direction, one of these bauds is for the A bit. The A bit is set to 1 when the S/T loop is in the fully activated state and is set to 0 at all other times. Thus, when the NT is transmitting INFO 2, the A bit is set to 0. When the NT is transmitting INFO 4, the A bit is set to 1.

### 3.12.4 SCP Nomenclature

There are seven nibble registers, 16 byte registers, and 10 overlay registers in the MC145574. These registers are accessed by means of the SCP. NR1(2) refers to nibble register 1, bit 2. Likewise, BR3(4) refers to byte register 3, bit 4, and OR5(6) refers to overlay register 5, bit 6.

The overlay registers are a second bank of registers available when the overlay register control bit BR15(7) is set to logic 1.

### 3.12.5 SCP Indication of Transmit and Receive States

Note that there are two SCP bits, BR11(5:4), used to signify what INFO state the MC145574 is receiving. In addition to this, BR11(3:2) are used to signify what INFO state the MC145574 is transmitting. Refer to Tables 9–2 and 9–3 for a detailed description of these bits.

# 4
# THE INTERCHIP DIGITAL LINK

## 4.1 INTRODUCTION

The Interchip Digital Link (IDL2) of the MC145574 is backwards compatible with the IDL of the MC145474/75 S/T transceiver of first generation. In addition to the standard operating mode, this enhanced interface features new modes that are programmable through the SCP.

The IDL2 is a four–wire interface used for full–duplex communication between ICs on the board level. The interface consists of a transmit path, a receive path, an associated clock, and a sync signal. These signals are known as $D_{out}$, $D_{in}$, DCL, and FSC, respectively. The clock determines the rate of exchange of data in both the transmit and receive directions, and the sync signal controls when this exchange is to take place. Three channels of data are exchanged every 8 kHz. These channels consist of two 64 kbps B channels and one 16 kbps D channel used for full–duplex communication between the NT and TE.

There are two modes of operation for an IDL2 device: IDL2 master and IDL2 slave. If an IDL2 device is configured as an IDL2 master, then FSC and DCL are outputs from the device. Conversely, if an IDL2 device is configured as an IDL2 slave, then FSC and DCL are inputs to the device. Ordinarily the MC145574 should be configured as an IDL2 slave when acting as an NT, and as an IDL2 master when acting as a TE. The exception to this rule is the option to configure the NT as an IDL2 master. The TE configured MC145574 also features the new option of operating in the IDL2 slave mode. These operation modes are described in Section 4.3.

## 4.2 SIGNAL DESCRIPTION

There are six pins associated with the IDL2 interface.

**FSC/FSR**

This pin is normally FSC and is an input/output pin to which all serial interface events are synchronized. This pin is periodic at 8 kHz. In the master mode, the pin is an output and is either derived from the S/T frame or from the XTAL. In the slave mode, this pin is an input.

FSC can be reconfigured through the SCP to be FSR. In this mode, the IDL2 operates with two independent frame syncs, one for the Tx direction (FST) and one for the Rx direction (FSR). FSR is bidirectional, the direction depending on whether the IDL2 is a master or a slave. See Register OR7 description.

**DCL**

This is an input/output pin that provides the clock to the serial interface. In the master mode, this pin is an output. In the slave mode, this pin is an input. The clock is continuous and the edges are synchronous with the frame sync.

When DCL is an output, the clock rate can be programmed through the SCP to be 2.56 MHz, 2.048 MHz, 1.536 MHz, or 512 kHz. When DCL is an input, the clock rate can be between 512 kHz and 4096 kHz (DCL should be a multiple of FSC.) Selection of the clock frequency is accomplished in the same manner as used in MC145474, through the bits BR7(2) and BR13(5). See Table 4–1 for IDL2 clock speeds.

**Table 4–1. IDL2 Clock Speeds**

| BR13(5) | BR7(2) | DCL |
|---|---|---|
| 0 | 0 | 2.56 MHz |
| 0 | 1 | 2.048 MHz |
| 1 | 0 | 1.536 MHz |
| 1 | 1 | 512 kHz |

**$D_{in}$**

This pin is always an input. Data to be output on the S/T–interface is input on this pin.

**$D_{out}$**

This pin is a three–state output. Data received on the S/T–interface is output on this pin during programmed timeslots and is high impedance at all other times.

**$\overline{TSEN}$/FST**

This pin is normally three–state, but it can be reconfigured through the SCP to be used as $\overline{TSEN}$ or FST. See Register OR7 description.

$\overline{TSEN}$ is an open drain output. $\overline{TSEN}$ can be used to enable an external bus driver and pulses low when data is being output on the $D_{out}$ pin. This signal can be used to control a high drive bus/backplane driver in applications where the $D_{out}$ data is going off–board. Since $\overline{TSEN}$ is open drain, it can be wire–OR'd with other devices and share the same driver.

This pin can also be reconfigured through the SCP to be used as FST. In this mode, the IDL2 interface operates with two independent frame syncs, one for the Tx direction (FST) and one for the Rx direction (FSR). FST is bidirectional, the direction depending on whether the IDL2 is a master or a slave.

**TFSC/TCLK/T_IN/FIX**

This pin is the FIX input in NT modes, but in the TE slave mode it is reconfigured to be used as TFSC and outputs an 8 kHz signal that is synchronized to the incoming S/T–interface frames. The TFSC can be used in NT2 applications where the TE slave mode is utilized. The TFSC can be used to synchronize the TE slaves to the network. Alternatively, this pin can output TCLK, selected via the SCP. TCLK is a clock whose frequency can be chosen via the SCP, which is also synchronized to the received S/T–interface. TCLK can be used as an alternative to TFSC in the NT2 slave–slave mode. Refer to the slave–slave mode section for further details on TFSC and TCLK. See Register OR7 description.

In the NT Terminal mode (NTTERM), this pin is T_IN. See the section on NT Terminal mode. See description for Register OR8.

## 4.3 IDL2 STANDARD MODE

### 4.3.1 NT IDL2 Slave

This is the normal mode of operation for the MC145574, when active as an NT. In this mode FSC and DCL are inputs to the device, and the outgoing S/T frame is synchronized to the IDL2 frame sync. Typically the MC145574, when configured as an NT, is situated on a line card or an NT1 box. As an IDL2 slave, this allows the S/T chip to derive its timing from the backplane or from the MC14LC5472/MC145572 U–chips. As mentioned previously, FSC must be 8 kHz, while DCL can be input to the device with any frequency from 512 kHz to 4.096 MHz.

When the MC145574 is configured as an NT, then BR7(3) determines whether the NT is acting as an IDL2 master or as an IDL2 slave. When BR7(3) is a 0, the MC145574, when acting as an NT, is behaving as an IDL2 slave. Conversely, when BR7(3) or OR8(3) is set to a 1, or when pulling high the M/$\overline{S}$ pin, the chip acting as an NT behaves as an IDL2 timing master.

### 4.3.2 NT IDL2 Master

As mentioned previously, the normal configuration for the MC145574, when configured as an NT, is as an IDL2 slave. However, in order to facilitate testing of the environment in which the MC145574 resides, the capability exists to configure the chip as an NT IDL2 master. In this mode of operation, the chip outputs FSC and DCL. These signals are divided down from the 15.36 MHz crystal input XTALIN and hence are synchronous with it. The NT IDL2 master mode also finds use in testing PC–based local area networks or in passive bus configurations. In these environments, it may be required to configure one of the TEs to act as an NT. The NT IDL2 master enables the user to do this. Writing a 1 to BR7(3) or OR8(3), or pulling high the M/$\overline{S}$ pin, puts the NT into the IDL2 master mode. Note that a software or a hardware reset reconfigures the NT as an IDL2 slave.

When the MC145574 is acting as an NT IDL2 master, the DCL can be programmed to output one of four frequencies. The DCL rate is determined by BR7(2) and BR13(5). In the NT IDL2 master mode, the DCL is obtained by dividing down from the 15.36 MHz crystal. Application of a software or a hardware reset will reset BR7(2) and BR13(5) to 0. Note that these bits have no application when the MC145574 is an NT IDL2 slave.

### 4.3.3 TE IDL2 Master

This is the normal mode of operation for the MC145574 when active as an NT. In this mode, the MC145574 derives its timing from the inbound data from the NT. When the TE is receiving either INFO 2 or INFO 4 from the NT, it adaptively phase–locks onto it. The TE sets the FSYNC bit (NR1(0)) high when this frame synchronization has been achieved. When this occurs, the TE outputs FSC, DCL, and $D_{out}$ synchronous with the inbound INFO 2 or INFO 4. If the TE is receiving INFO 2, it outputs “idle 1s” on $D_{out}$ in the B1, B2, and D channel timeslots. If the TE is receiving INFO 4, it outputs valid data in these timeslots.

Note that when the TE has reached its fully active state, it internally sets the activate indication bit (NR1(3)). (The active state for a TE is when it is receiving INFO 4 from the NT, has phase–locked onto it, and is transmitting back INFO 3 to the NT.) In the TE IDL2 master mode, BR7(2) and BR7(3) determine the output DCL rate. See description of BR7 bits 1 and 2 in Section 9.9.

### 4.3.4 TE IDL2 Master Free Run

The capability exists in the MC145574 to configure the chip as a TE operating in the IDL2 master free run mode. This is done by setting BR7(3) to a 1. In this mode, the TE sends out a DCL and FSC regardless of the state of the frame synchronization bit (NR1(0)). If NR1(0) is low, then FSC and DCL are derived from the crystal in the same way as in the NT IDL2 master mode. Upon achieving frame synchronization (i.e., the TE is receiving either INFO 2 or INFO 4 from the NT, has phase–locked onto it, and has set NR1(0)), FSC and DCL will become synchronous to the inbound INFO 2 or INFO 4 from the NT. The TE IDL2 master mode has the capability of providing four clock rates: 2.56 MHz, 2.048 MHz, 1.536 MHz, and 512 kHz.

### 4.3.5 TE IDL2 Slave

The TE slave–slave mode should be selected when the device is to be used on the T–interface of an NT2. In this mode, the IDL2 is in the slave mode, and D channel data is continuously transmitted/received to/from the T–interface. The D channel access algorithm is disabled in this mode.

In this mode, the frame sync and serial clock are inputs. The IDL2 circuitry incorporates buffering to accommodate any phase relationship between the frame sync and the received S/T frame. The buffering is able to absorb low–frequency wander between the IDL2 frame sync and the S/T frame. The wander absorption capability exceeds the requirement of Q.502, which defines wander as 18 μs peak–to–peak at frequencies below 10 Hz over a 24–hour period.

## 4.3.6 Additional Notes

### 4.3.6.1 Phase Relationship of the NT Transmit Signal with Respect to FSC/FSR

The MC145574 operating as an NT behaves as an IDL2 slave, FSC/FSR and DCL being inputs to the device. FSC/FSR is a single positive polarity pulse, one DCL cycle in duration, and is periodic at an 8 kHz rate. The MC145574 operating as an NT uses FSC/FSR to correctly position its outbound waveform. Thus, the FSC/FSR input to the NT and the NT's outbound INFO 2 or INFO 4 are synchronous. The phase relationship of these signals is shown in Figure 4–1 with a "close–up shot" included.

### 4.3.6.2 Phase Relationship of the TE Transmit Signal with Respect to FSC/FSR, When in the IDL2 Master Mode

The MC145574 operating as a TE behaves as an IDL2 master; FSC/FSR and DCL are outputs from the device. The TE derives its timing from the inbound INFO 2 or INFO 4 from the NT. There is a two–baud turnaround in the TE in accordance with CCITT I.430, ETSI ETS 300012, and ANSI T1.605 specifications; i.e., the time between the TE's received "F bit" and its transmitted "F bit" is equivalent to two bauds. This is indicated in Figure 4–2. The TE outputs FSC/FSR, DCL, and $D_{out}$ when it has achieved frame synchronization. The phase relationship of the TE's transmitted INFO 3 and FSC/FSR is as shown in Figure 4–3 with a "close–up shot" included.

### 4.3.6.3 Operation of Multiple MC145574s in TE Slave Mode

When the MC145574 is configured for TE slave mode in NT2 applications, the T_IN/TFSC/TCLK/FIX pin defaults to the TFSC function. As TFSC, this pin outputs an 8 kHz frame sync that is synchronized to recovered timing from the network.

In TE slave mode, the T_IN/TFSC/TCLK/FIX pin function can be changed to TCLK, which outputs a network synchronized high frequency clock. This is done by setting OR7(5) to a 1. The clock frequency of TCLK is selected in the same manner as programming the DCL clock in IDL2 master mode.

Elastic buffers are included in TE slave mode to allow the MC145574 to operate with any phase relationship between the IDL2 frame sync and the network. This buffer also allows the frame sync to wander with respect to the network, up to 60 μs peak–to–peak. This exceeds the requirements of Q.502, which states that wander up to 18 μs peak–to–peak may arise over a 24–hour period.

An example architecture of an NT2 is shown in Figure 4–4. The TFSC or TCLK signal supplied by the TE is used to synchronize the entire NT2 to the network. The TFSC/TCLK pins can be wire OR'd together and connected to $V_{DD}$ via a pull–up resistor. Each TE looks at the TFSC/TCLK pin during its programmed B1 channel timeslot. If there is no signal present and the TE is activated, it outputs a synchronized signal on TFSC/TCLK. It is important for all TEs to have their B and D channels configured using the timeslot assigner, and no two devices can share a timeslot.

### 4.3.6.4 Independent Tx/Rx Frame Syncs

Via the SCP, two pins (FST and FSR) are available to handle the transmit and receive frames independently on the IDL2 interface. These pins must operate synchronously with the DCL clock. Operation of FST and FSR is dependent on the master or slave mode. Separate frame syncs are enabled by setting OR7(4) to a 1.

In the slave mode, FST and FSR may assume any relationship with respect to each other.

In the master mode, both FST and FSR are operational and locked together in time. Long frame format can not be used with independent Tx/Rx frame syncs.

### 4.3.6.5 Timeslot Assignment

The MC145574 contains a timeslot assigner. The timeslot immediately following the FSC/FSR/FST signal is timeslot zero. Timeslots are available up to the maximum DCL rate of 4096 kHz. The timeslots are programmed through a group of control registers in the overlay register map. Up to 256 start times may be defined, corresponding to each 2–bit boundary defined by DCL.

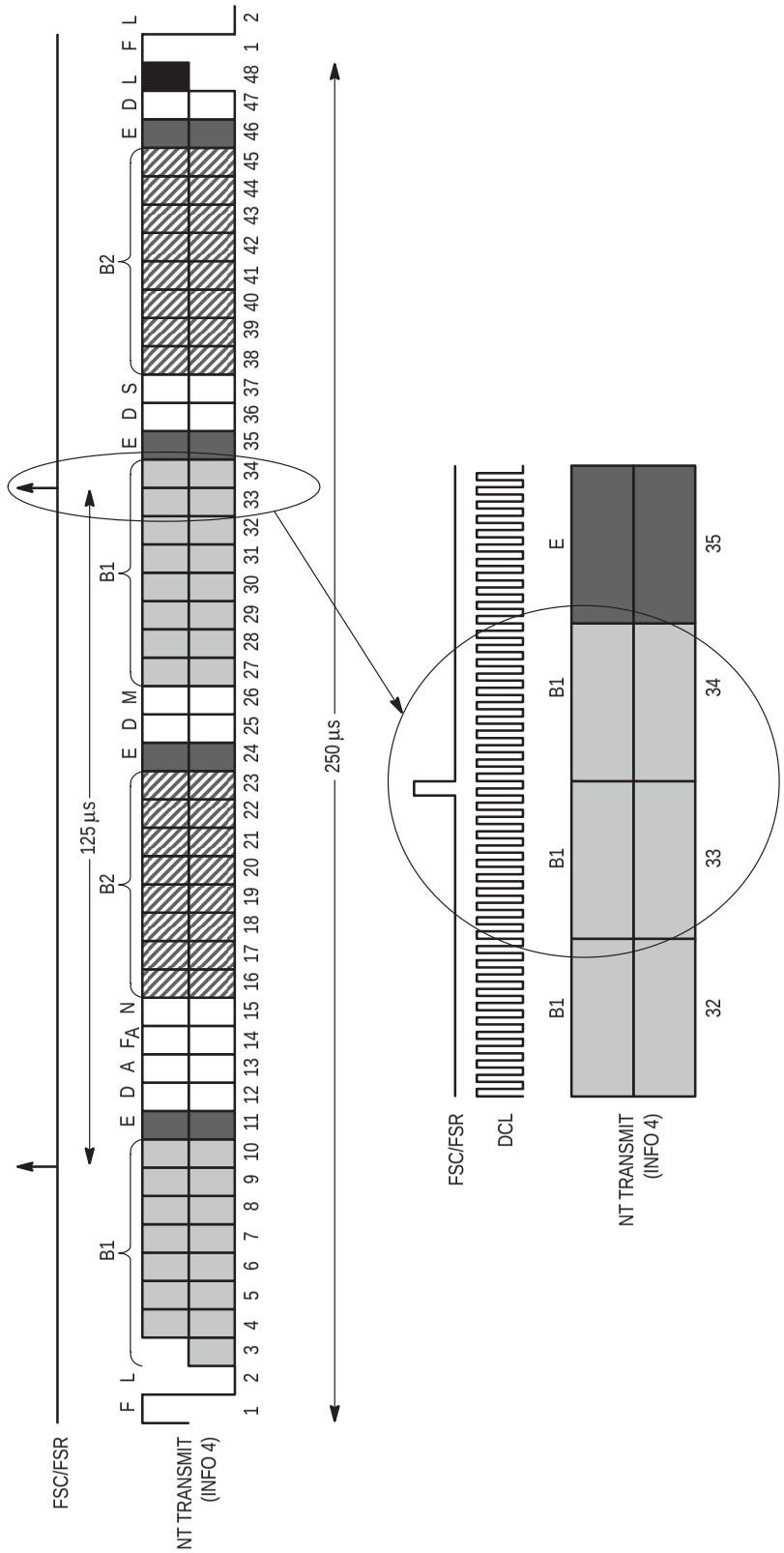



**Figure 4–1. Phase Relationship of NT Transmit Signal**

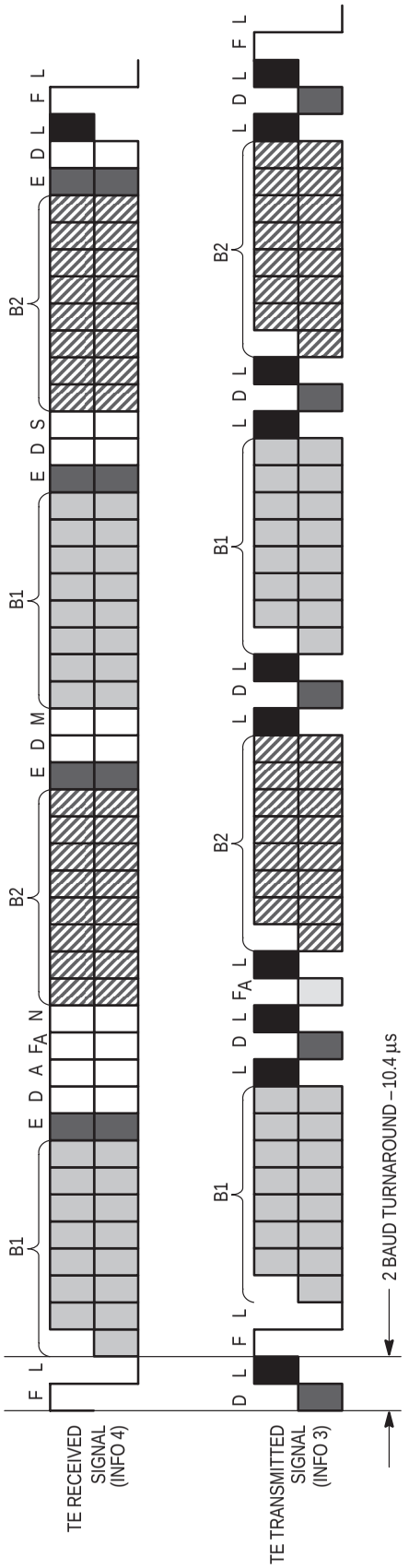



**Figure 4–2. Two–Baud Turnaround in TE**

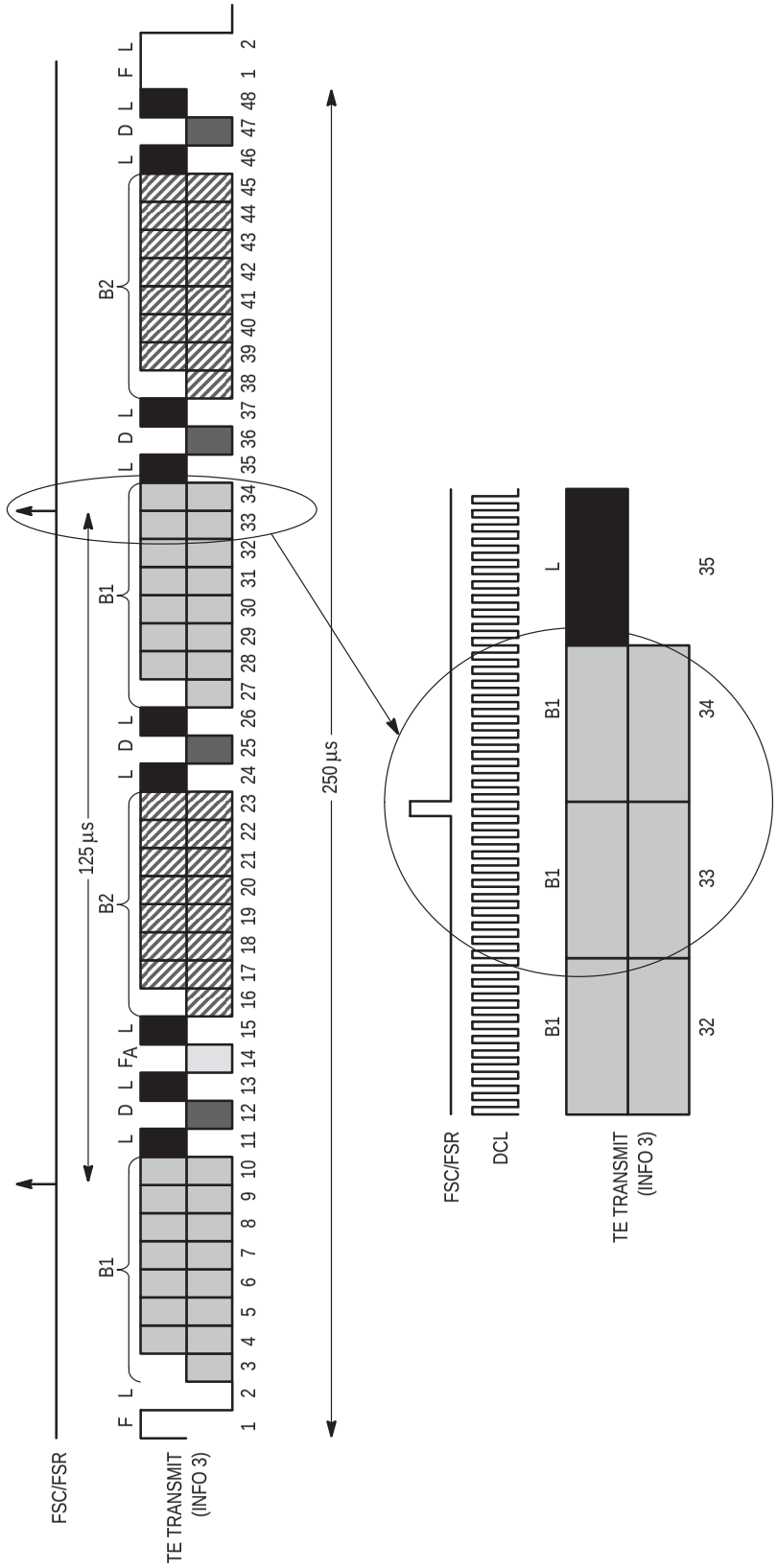



**Figure 4–3. Phase Relationship of TE Transmit Signal**

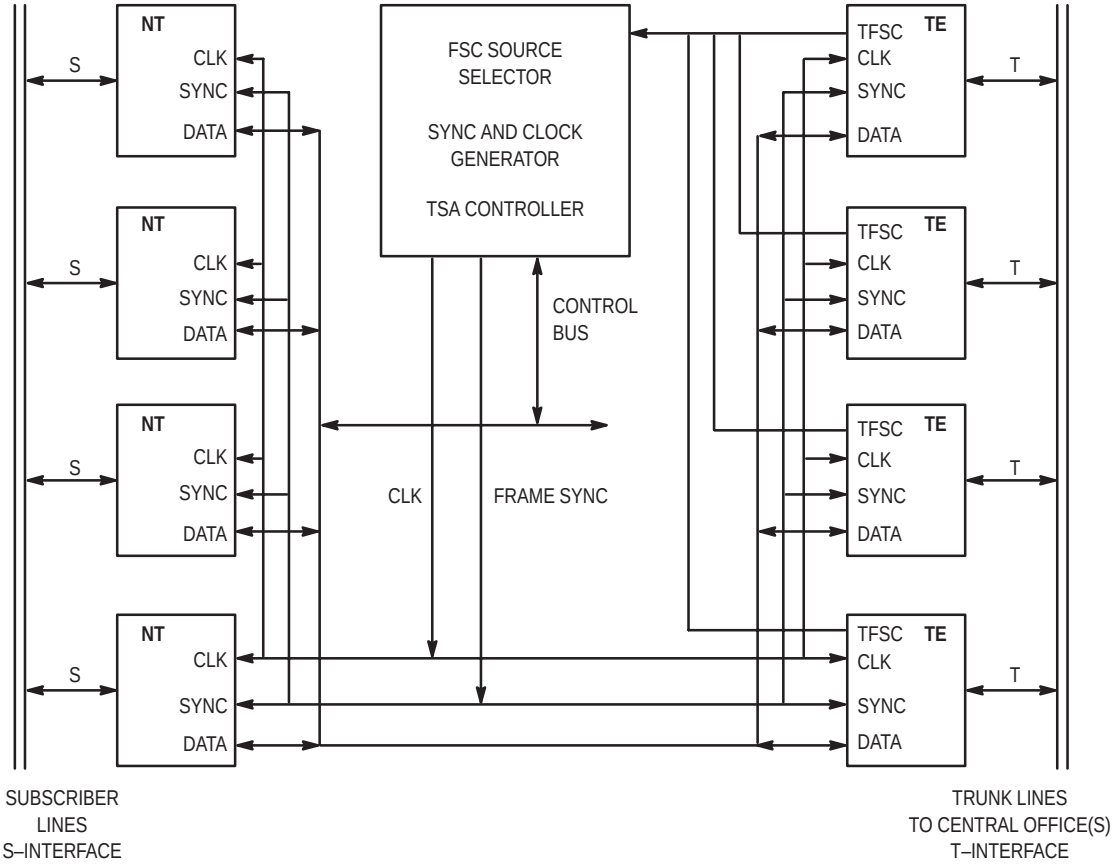



**Figure 4–4. Example Architecture of an NT2**

Independent timeslot assignment is available for the B1, B2, and D channels in both the transmit and receive directions. B1, B2, and D timeslots may be enabled separately. When a timeslot is enabled, the IDL2 automatically enters timeslot mode. If any one channel's timeslot is not enabled, data transmitted by the framer for that channel will be filled with all ones, and the channel will not be present on $D_{out}$.

With a DCL rate of 4096 kHz, it is possible to allocate 1 of 256 possible timeslots to each data channel. It is important that the software selects a timeslot consistent with the DCL rate. When a clock rate of 2048 kHz is being used, only 128 timeslots are available. If a timeslot out with the available range is chosen, then no data transfer occurs for that timeslot.

The default values assigned to the B1, B2, and D channels are 00H, 04H, and 08H. These values provide an IDL2 8–bit output format as default.

The IDL2 10–bit mode is not available when the timeslot assigner has been enabled.

**CAUTION**

Do not program overlapping timeslots even if a timeslot has not been enabled. The transmit and receive timeslot for a given B1, B2, or D channel can be the same.

#### 4.3.6.6 Short and Long Framing

In master timing mode, the default state is to supply a one–clock–wide FSC/FSR/FST frame sync. However, an option is provided to change this to long frame. The length of the long frame pulse is always 8–bit clocks, regardless of whether an 8– or 10–bit format is selected. In the slave mode, the MC145574 will automatically adjust to whichever framing method is supplied. If the frame sync is two or more clocks wide, the MC145574 assumes a long frame format.

A long frame format cannot be used in timeslot assignment mode.

#### 4.3.6.7 $\overline{\text{TSEN}}$ Signal

The $\overline{\text{TSEN}}$ signal is enabled via the SCP. See description for OR7 bits 1 and 0. This pin then becomes an open drain output that pulls low when data is being output from $D_{out}$. This signal can then be used to enable an external driver in applications where the IDL2 data goes off–board, such as PBXs, channel banks, etc.

#### 4.3.6.8 Miscellaneous

**Clock Options**

In the slave mode, the IDL2 interface accepts any clock from 512 kHz to 4096 kHz in 8 kHz increments.

In the master mode, the DCL has four frequency options, programmable through the SCP. The clock rate can be either 2.56 MHz, 2.048 MHz, 1.536 MHz, or 512 kHz. The default selection is 2.56 MHz.

**B Channel Exchange**

An option is provided to exchange the B1 and B2 channels inside the IDL2. This exchange operates simultaneously in both Tx and Rx directions.

**B1 and B2 Blocking**

Options are provided to independently block or force the B1 and B2 channels to all ones in both the transmit and receive directions.

**B1 and B2 Inversion**

Options are provided to independently invert the B1 and B2 channels in both the transmit and receive directions.

**B1, B2, and D Loopbacks**

Options are provided to make an individual loopback on each B1, B2, or D channel.

#### 4.3.6.9 IDL2 Waveform Diagrams

The relative timing relationships of the IDL2 signals are shown in Figures 4–5 through 4–8.

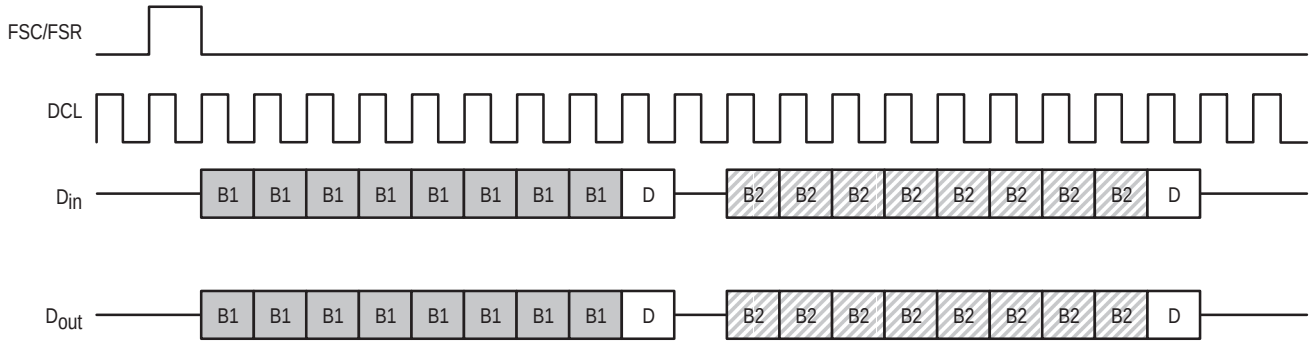



**Figure 4–5. Standard IDL2 10–Bit Mode**

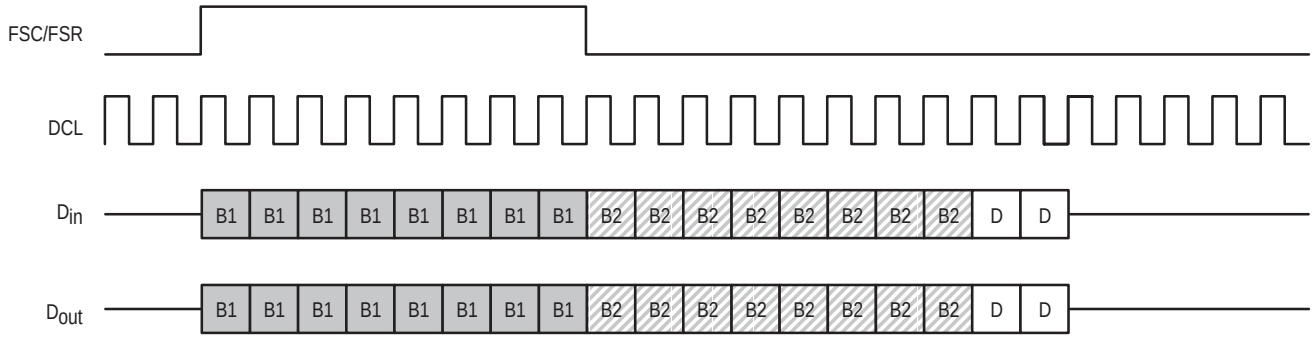



**Figure 4–6. Standard IDL2 8–Bit Mode with Long Frame Sync**

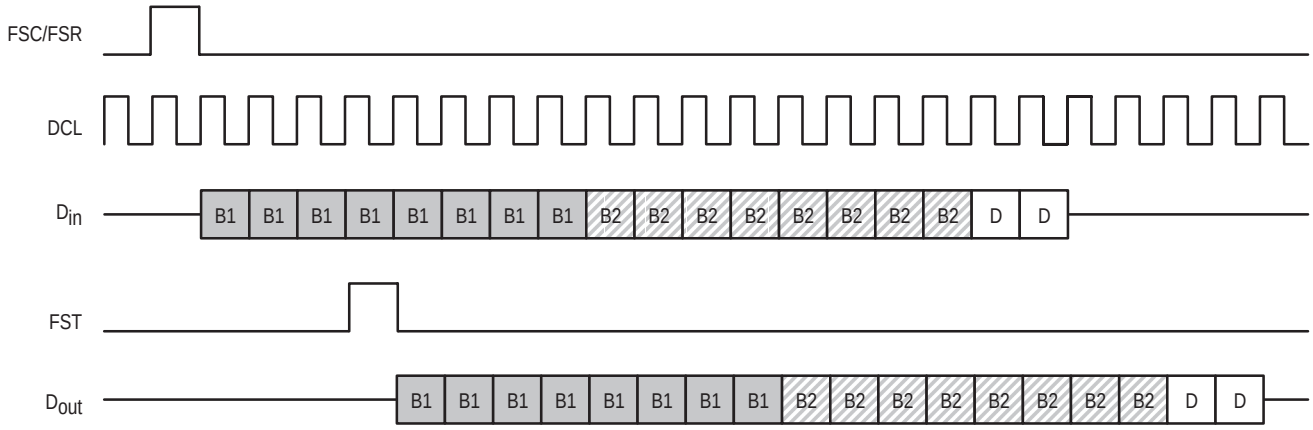



**Figure 4–7. Standard IDL2 8–Bit Slave Mode with Independent Frame Syncs**

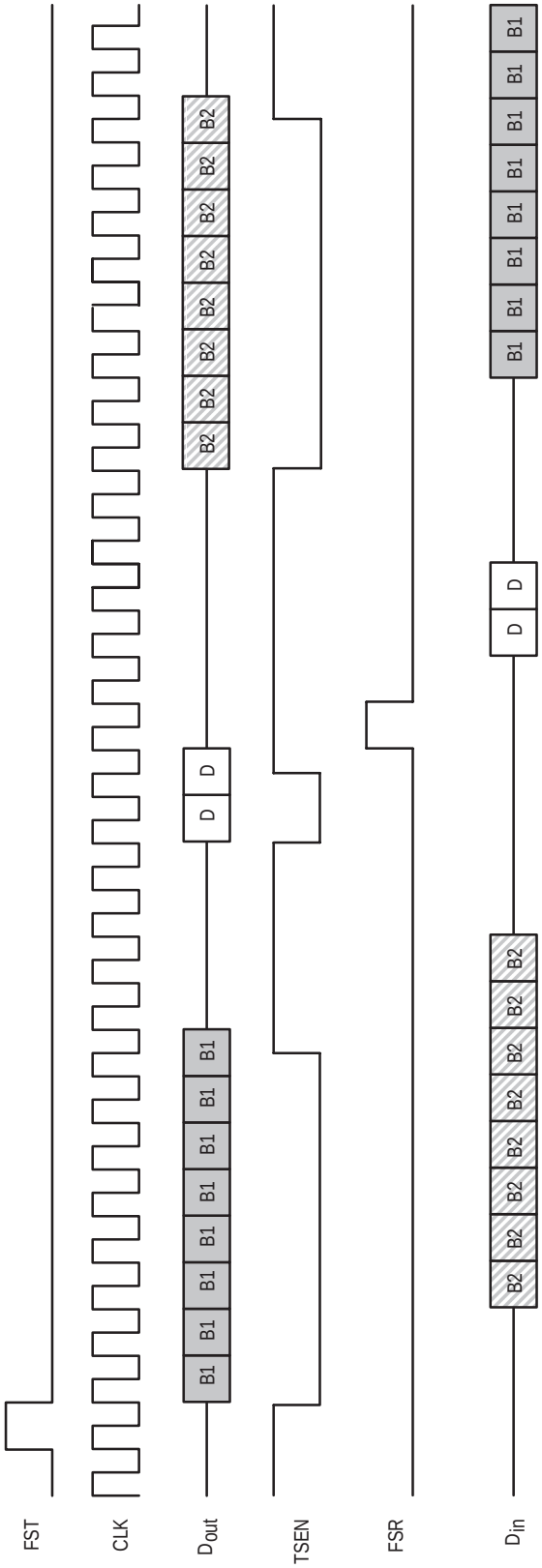



**Figure 4–8. Timeslot Operation with Independent Slave Frame Syncs, $\overline{\text{TSEN}}$**

# 5
# SERIAL CONTROL PORT

## 5.1 INTRODUCTION

The MC145574 is equipped with a serial control port (SCP). This SCP is used by external devices (such as an MC145488 DDLC or 68302) to communicate with the S/T transceiver. The SCP is an industry standard serial control port and is compatible with Motorola's SPI, which is used on several single–chip MCUs.

The SCP is a five–wire bus with control and status bits, with data being passed to and from the S/T transceiver in a full–duplex fashion.

The SCP interface consists of a transmit path, a receive path, an associated clock, an enable signal, and an interrupt indicate. These signals are known as SCP Tx, SCP Rx, SCPCLK, $\overline{\text{SCPEN}}$, and $\overline{\text{IRQ}}$.

The clock determines the rate of exchange of data in both the transmit and receive directions, the enable signal governs when this exchange is to take place, and the interrupt signal indicates that an interrupt condition exists and a read operation of the interrupt status register (NR3) is required.

The operation/configuration of the S/T transceiver is programmed by setting the state of the control bits within the S/T transceiver. The control, status, and data information reside in eight 4–bit–wide nibble registers, sixteen 8–bit–wide byte registers, and sixteen 8–bit–wide overlay registers. The nibble registers are accessed via an 8–bit SCP bus transaction. The 16–byte–wide registers are accessed by first writing to a pointer register within the eight 4–bit–wide nibble registers. This pointer register (NR(7)) then contains the address of the byte wide register to be read from or written to on the following SCP transaction. Thus, an SCP byte access is in essence a 16–bit operation. Note that this 16–bit operation can take place by means of two 8–bit accesses or a single 16–bit access.

## 5.2 SCP TRANSACTIONS

There are six types of SCP transactions.

1. SCP Nibble Register Read
2. SCP Nibble Register Write
3. SCP Byte Register Read
4. SCP Byte Register Write
5. SCP Merged Read
6. SCP Merged Write

The following sections contain a discussion on each type of SCP transaction.

### 5.2.1 SCP Nibble Register Read

A nibble register read is an 8–bit SCP transaction. Figure 5–1 illustrates this process. To initiate an SCP nibble register read, the $\overline{\text{SCPEN}}$ pin is brought low. Following this, a read/$\overline{\text{write}}$ (R/$\overline{\text{W}}$) bit, followed by three primary address bits (A0 – A2 = 0 to 6), are shifted (MSB first) into an intermediate buffer register on the first four rising edges of SCPCLK, following the high–to–low transition of $\overline{\text{SCPEN}}$. If a read operation is to be performed, then R/$\overline{\text{W}}$ should be a 1. The three address bits clocked in after the R/$\overline{\text{W}}$ bit select which nibble register is to be read. The contents of this nibble register are shifted out on SCP Tx on the subsequent four falling edges of SCPCLK; i.e., the four falling edges of SCPCLK after the rising edge of SCPCLK, which clocked in the last address bit (LSB). $\overline{\text{SCPEN}}$ should be brought

back high after the transaction, before another rising edge of SCPCLK is encountered. Note that SCP Rx is ignored during the time that SCP Tx is being driven. Also note that SCP Tx comes out of high impedance only when it is transmitting data.

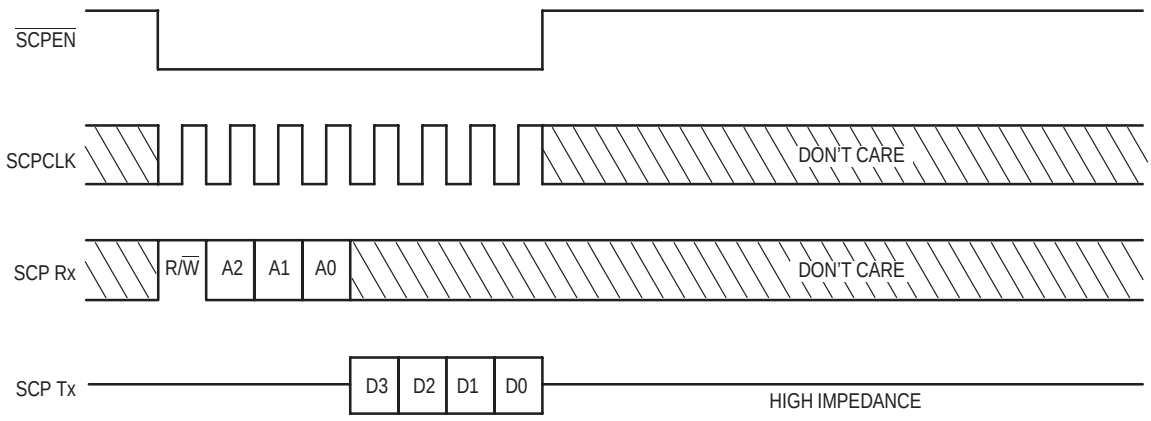
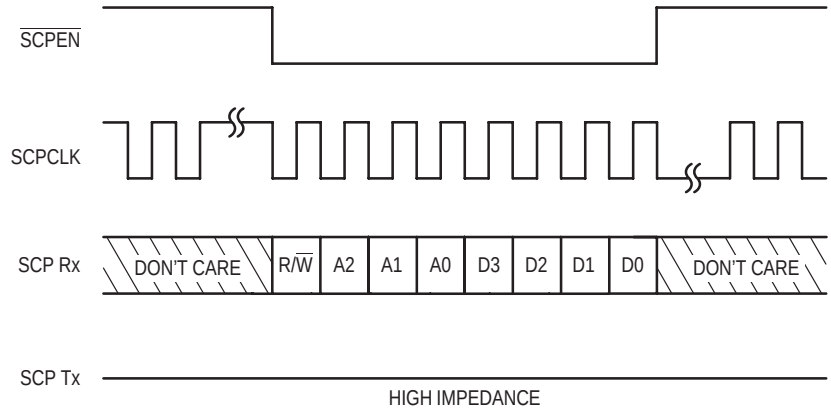



**Figure 5–1. Serial Control Port Nibble Register Read Operation**

## 5.2.2 SCP Nibble Register Write

A nibble register write is an 8–bit SCP transaction. Figure 5–2 illustrates this process. To initiate an SCP nibble register write, the $\overline{\text{SCPEN}}$ pin must be brought low. Following this, an R/$\overline{\text{W}}$ bit followed by three primary address bits are shifted (MSB first) into an intermediate buffer register on the first four rising edges of SCPCLK following the high–to–low transition of $\overline{\text{SCPEN}}$. If a write operation is to be performed, then R/$\overline{\text{W}}$ should be a 0. The three address bits, clocked in after the R/$\overline{\text{W}}$ bit, select the nibble register to be written to. The data shifted in on the next four rising edges of SCPCLK is then written to the selected register. Throughout this whole operation the SCP Tx pin remains in high–impedance state. Note that if a selected register or bit in a selected register is “read only”, then a write operation has no effect.

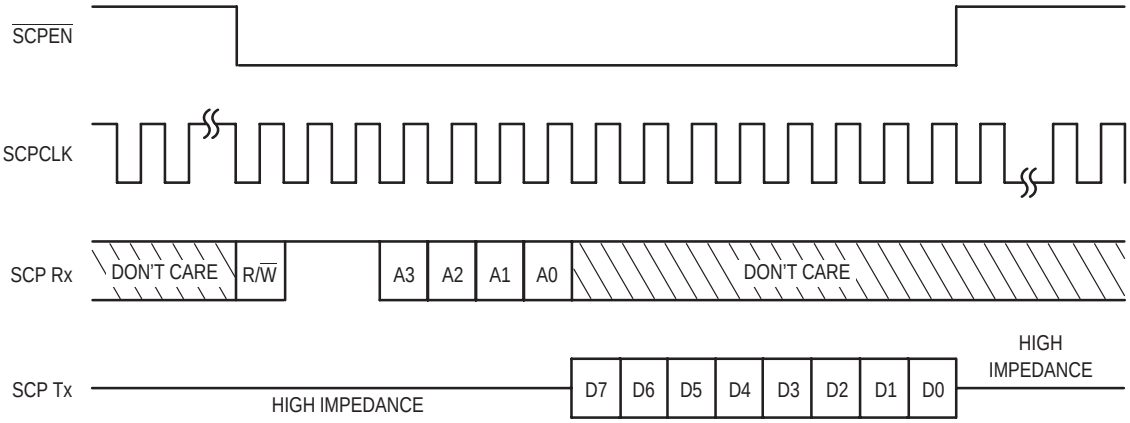



NOTES:
1. R/$\overline{\text{W}}$ = 0 for a read operation.
2. Data is shifted out on SCP Tx on the falling edges of SCPCLK, MSB first.
3. Data is shifted into the chip from SCP Rx on the rising edges of SCPCLK, MSB first.
4. A2, A1, A0 = 0 to 6.

**Figure 5–2. Serial Control Port Nibble Register Write Operation**

### 5.2.3 SCP Byte Register Read

A byte register read is a 16–bit SCP transaction. Figure 5–3 illustrates this process. To initiate an SCP byte register read, the $\overline{\text{SCPEN}}$ is brought low. Following this, an R/$\overline{\text{W}}$ bit is shifted in from SCP Rx on the next rising edge of SCPCLK. This bit determines the operation to be performed; read or write.




NOTES:
1. R/$\overline{\text{W}}$ = 1 for a read operation.
2. Data is shifted out on SCP Tx on the falling edges of SCPCLK, MSB first.
3. Data is shifted into the chip from SCP Rx on the rising edges of SCPCLK, MSB first.

**Figure 5–3. Serial Control Port Byte Register Read Operation**

If R/$\overline{\text{W}}$ is a 1, then a read operation is selected. Conversely, if R/$\overline{\text{W}}$ is a 0, then a write operation is selected. The next three bits shifted in from SCP Rx on the three subsequent rising edges of SCPCLK are primary address bits (A0 – A2 = 7), as mentioned previously. With all three bits equal to 1, nibble register 7 (NR7) is selected. This is a pointer register, the selection of which informs the device that a byte operation is to be performed. When NR7 is selected, the following four bits shifted in from SCP Rx on the following four rising edges of SCPCLK are automatically written to NR7. These four bits are the address bits for the byte operation. In a read operation, the next eight falling edges of SCPCLK shift out the data from the selected byte register on SCP Tx.

As mentioned previously, an SCP byte access is a 16–bit transaction. This can take place in one 16–bit exchange or two 8–bit exchanges. If the transaction is performed in two 8–bit exchanges, the $\overline{\text{SCPEN}}$ should be returned high after the first eight bits have been shifted into the part.

When $\overline{\text{SCPEN}}$ comes low again, the MSB of the selected byte presents itself on SCP Tx. The following seven falling edges of SCPCLK shift out the remaining seven bits of the byte register. Note that the order in which data is written into the part and read out of the part is independent of whether the byte access is done in one 16–bit exchange or in two 8–bit exchanges. Figure 5–4 illustrates this process.

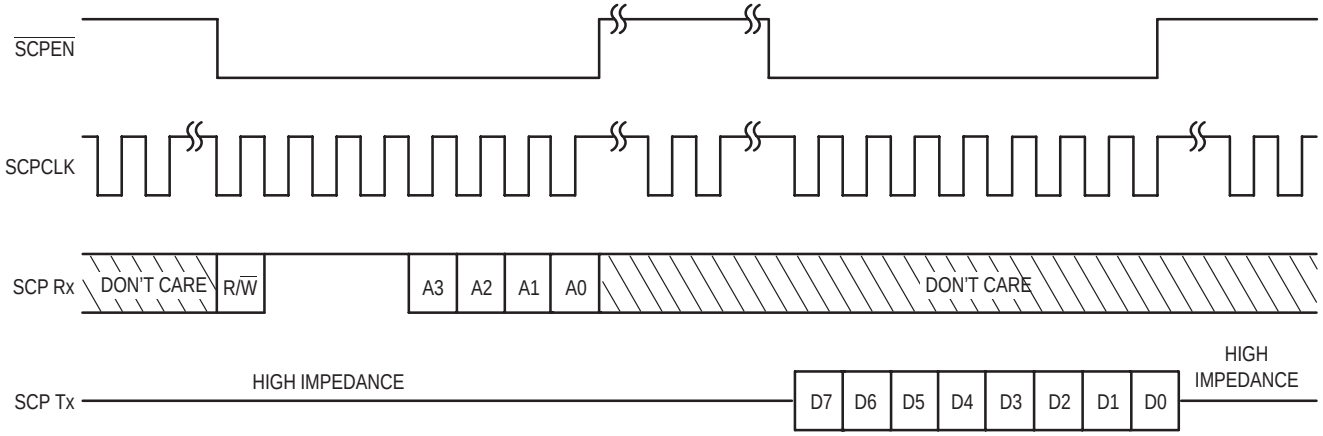
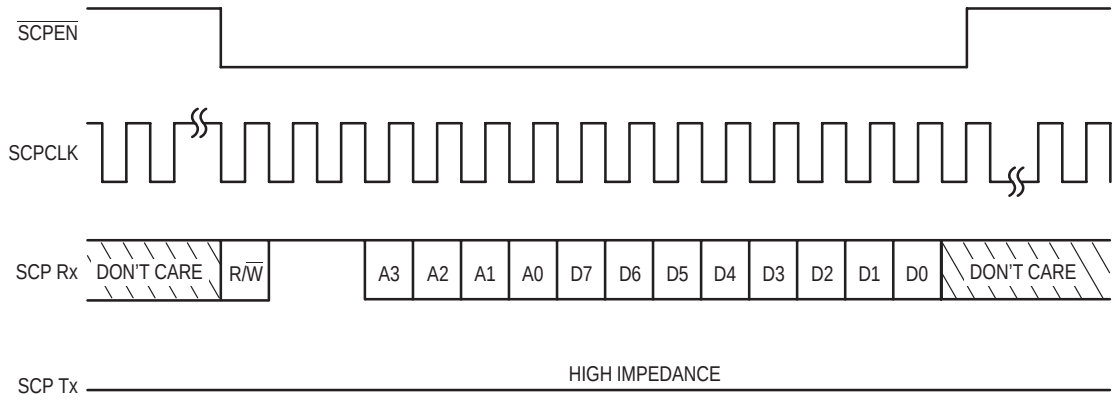



**Figure 5–4. Serial Control Port Byte Register Read Operation Double 8–Bit Transaction**

## 5.2.4 SCP Byte Register Write

A byte register write is also a 16–bit SCP transaction. Figure 5–5 illustrates this process. To initiate an SCP byte register write, the $\overline{\text{SCPEN}}$ must be brought low. As before, the next bit determines whether the operation is to be read or write. If the first bit is a 0, then a write operation is selected. Again the next three bits read in from SCP Rx on the subsequent three rising edges of SCPCLK must all be 1 in order to select the pointer nibble register (NR7). The following four bits shifted in are automatically written into NR7. As in an SCP byte register read, these bits are the address bits for the selected byte register operation. The next eight rising edges of SCPCLK shift in the data from the SCP Rx. This data is then stored in the selected byte register. Throughout this operation SCP Tx is in a high–impedance state. Note that if the selected byte is "read only", then this operation has no effect.




NOTES:
1. R/$\overline{\text{W}}$ = 1 for a read operation.
2. Data is shifted out on SCP Tx on the falling edges of SCPCLK, MSB first.
3. Data is shifted into the chip from SCP Rx on the rising edges of SCPCLK, MSB first.

**Figure 5–5. Serial Control Port Byte Register Write Operation**

As mentioned previously, an SCP byte access is a 16–bit transaction. This can take place in one 16–bit exchange or two 8–bit exchanges. If the transaction is performed in two 8–bit exchanges, then $\overline{\text{SCPEN}}$ should be returned high after the first eight bits have been shifted into the part.

When $\overline{\text{SCPEN}}$ comes low again, the next eight rising edges of SCPCLK shift data in from SCP Rx. This data is then stored in the selected byte. Figure 5–6 illustrates this process.

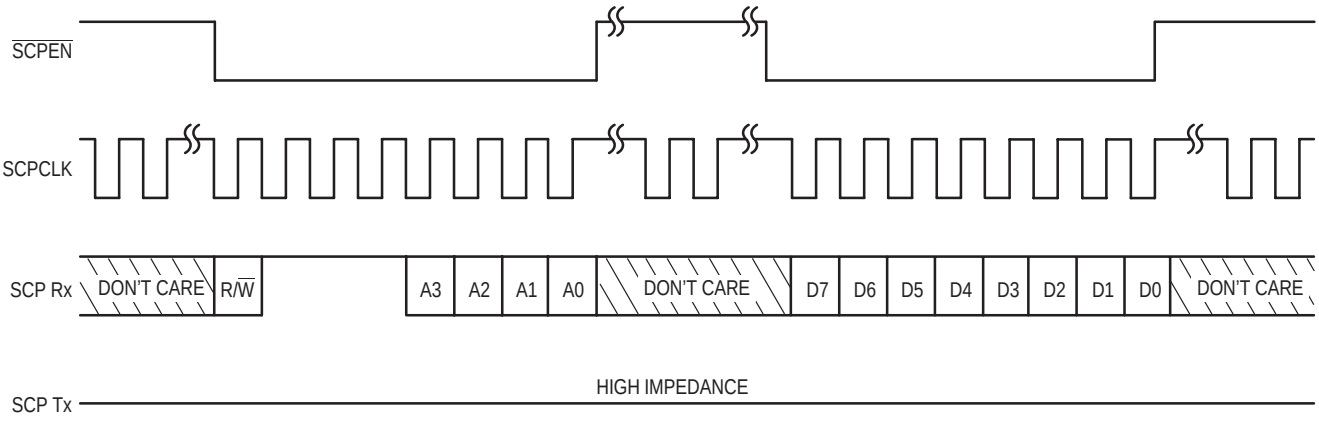
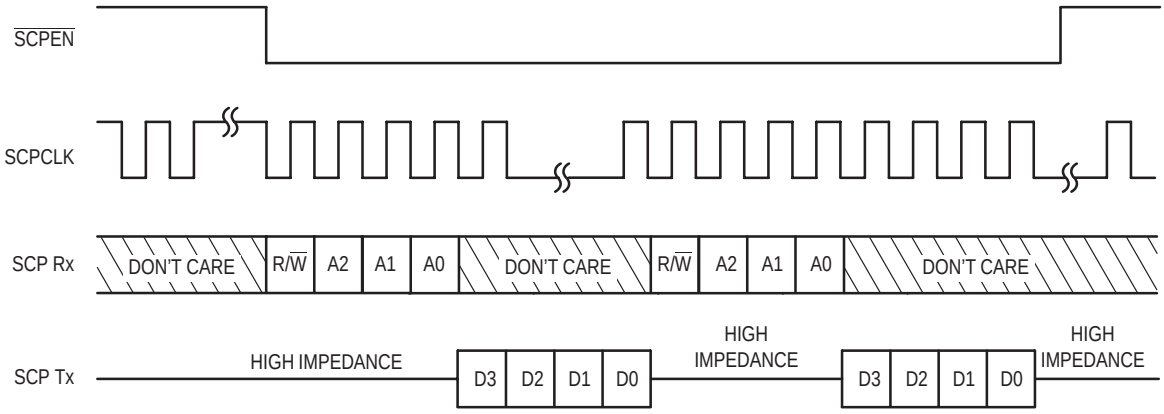



**Figure 5–6. Serial Control Byte Register Write Operation Double 8–Bit Transaction**

## 5.2.5 SCP Merged Read/Write

Merged operations are accomplished by not taking $\overline{\text{SCPEN}}$ high between separate SCP instructions. The SCP bytes/nibbles are strung together in a continuous bit stream and can be a mux or read/write command. The device is able to extract the separate instructions and provide the appropriate response. The $\overline{\text{SCPEN}}$ signal goes low at the start of the bit stream and goes high again at the end.

Figure 5–7 illustrates this process with two consecutive nibble register read operations. The merged instructions can be a free mix of nibble/byte/read/write operations.




NOTES:
1. R/$\overline{\text{W}}$ = 1 for a read operation.
2. Data is shifted out on SCP Tx on the falling edges of SCPCLK, MSB first.
3. Data is shifted into the chip from SCP Rx on the rising edges of SCPCLK, MSB first.

**Figure 5–7. Merged Serial Control Port Nibble Register Read Operation**

## 5.3 SIGNAL DESCRIPTION

There are five signals which constitute the SCP bus.

1. SCP Tx
2. SCP Rx
3. SCPCLK
4. $\overline{\text{SCPEN}}$
5. $\overline{\text{IRQ}}$

A description of each signal follows.

### 5.3.1 SCP Tx

SCP Tx is used to output control, status, and data information from the MC145574 S/T transceiver. The data is output in either 4–bit nibble or 8–bit byte groupings. The data is output in 4–bit nibble groupings during a nibble register read and in 8–bit byte groupings during a byte register read. Data is shifted out on SCP Tx on the falling edges of SCPCLK, MSB first.

In a nibble register read transaction, the fourth rising edge of SCPCLK after $\overline{\text{SCPEN}}$ goes low shifts the LSB of the 3–bit nibble address into the MC145574. The following falling edge of SCPCLK shifts out the first bit of the selected nibble register (MSB) and takes SCP Tx out of the high–impedance state. The next three falling edges of SCPCLK shift out the other three bits of the selected nibble register. When the last bit (LSB) has been shifted out, $\overline{\text{SCPEN}}$ should be returned high. This action returns SCP Tx to a high–impedance state.

In a byte register read transaction, the eighth rising edge of SCPCLK after $\overline{\text{SCPEN}}$ goes low shifts in the LSB of the 4–bit byte address. The following falling edge of SCPCLK (provided $\overline{\text{SCPEN}}$ is still low) shifts out the first bit (MSB) of the selected byte register and takes SCP Tx out of high impedance. The next seven falling edges of SCPCLK shift out the remaining seven bits of the selected byte register. When the last bit (LSB) has been shifted out, $\overline{\text{SCPEN}}$ should be returned high. This action returns SCP Tx to a high–impedance state.

### 5.3.2 SCP Rx

SCP Rx is used to input control, status, and data information to the S/T transceiver. Data is shifted into the device on rising edges of SCPCLK. The format for the input of data is as follows: the first bit is the R/$\overline{\text{W}}$ bit (1 = read, 0 = write). This bit selects the operation to be performed on the selected registers within the MC145574 S/T transceiver. The next three bits address one of eight specific nibble registers within the MC145574 S/T transceiver on which the read or write operation is to be performed. The address bits are shifted in MSB first. The last four bits are either the data bits (MSB first) that are to be written to the S/T transceiver nibble register (NR0 through NR6), or are four additional address bits (if NR7 had been addressed). These address bits select one of the 16–byte–wide registers (which are accessed during the next eight cycles of the SCPCLK or a second 8–bit access). SCP Rx is ignored when data is being shifted out on SCP Tx, or when $\overline{\text{SCPEN}}$ is high.

### 5.3.3 SCPCLK

This is an input to the device used for controlling the rate of transfer of data into and out of the SCP. Data is shifted into the part from SCP Rx on rising edges of SCPCLK. Data is shifted out of the part on SCP Tx on falling edges of SCPCLK. SCPCLK can be any frequency up to 4.096 MHz.

An SCP transaction takes place when $\overline{\text{SCPEN}}$ is brought low. Note that SCPCLK is ignored when $\overline{\text{SCPEN}}$ is high; i.e., it may be continuous or it can operate in the burst mode.

### 5.3.4 $\overline{\text{SCPEN}}$

This signal, when held low, selects the SCP for the transfer of control, status, and data information into and out of the MC145574 S/T transceiver. $\overline{\text{SCPEN}}$ should be held low for 8 or 16 periods of the SCPCLK signal, in order for information to be transferred into or out of the MC145574 S/T transceiver. The phase relationship of $\overline{\text{SCPEN}}$, with respect to SCPCLK, is as shown in Figures 5–1 through 5–6 inclusive.

The transition of $\overline{\text{SCPEN}}$ going high will abort any SCP operation in progress, and will force the SCP Tx pin into the high–impedance state.

### 5.3.5 $\overline{\text{IRQ}}$

$\overline{\text{IRQ}}$ is an open drain output to the device used for indicating that an interrupt condition exists. This pin is normally pulled high by an external resistor. When this pin goes low, it indicates a read operation of the interrupt status register (NR3) is required.

## 5.4 SCP HIGH-IMPEDANCE DIGITAL OUTPUT MODE (SCP HIDOM)

The MC145574 S/T transceiver has the capability of forcing all output pins of the MC145574 (both analog and digital) to the high–impedance state. This feature, known as the “Serial Control Port High–Impedance Digital Output Mode”, or SCP HIDOM, is provided to allow “in circuit” testing of other circuits or devices resident on the same PCB, without requiring the removal of the MC145574.

The SCP HIDOM mode is entered by holding $\overline{\text{SCPEN}}$ low for a minimum of 33 consecutive rising edges of SCPCLK while SCP Rx is high. After entering this mode, if $\overline{\text{SCPEN}}$ goes high or if SCP Rx goes low, the device will exit the SCP HIDOM mode and return to normal operation.

## 5.5 ADDITIONAL NOTES

### 5.5.1 SCP Independent of Crystal

The MC145574 S/T transceiver operates with a 15.36 MHz crystal frequency. Details of the crystal circuit can be found in Section 7. The SCP operates independently of the 15.36 MHz crystal; i.e., the SCP can be accessed in the presence or absence of the 15.36 MHz input.

### 5.5.2 SCP Slave

The SCP in the MC145574 always operates in the SCP slave mode. The SCP slave mode is defined as having SCPCLK and $\overline{\text{SCPEN}}$ as inputs to the device. Thus, any device which communicates with the MC145574 via the SCP must be able to operate in the SCP master mode where SCPCLK and $\overline{\text{SCPEN}}$ are outputs. Note that the MC145488 dual data link controller (DDLC) and 68302 operate in the SCP master mode.

# 6
# GENERAL CIRCUIT INTERFACE

## 6.1 OVERVIEW

The MC145574 is able to work with a General Circuit Interface port (GCI). The GCI is a standard four–wire interface between devices for the subscriber access in ISDN and analog environments. The principle use in these applications is to control the subscriber line interface circuitry.

The following are some of the benefits of the General Circuit Interface.

- Operation and Maintenance Features
- Activation and Deactivation Facilities (via a Control Indication (C/I) Channel)
- Well–Defined Transmission Protocols to Ensure Correct Information Transfer Between GCI Compatible Devices
- Point–to–Point and Multipoint Communication Links
- Multiplexed Mode of Operation Where up to Eight GCI Channels can be Combined to Form a Single Data Stream

The GCI interface consists of a transmit path, a receive path, an associated clock, and a frame sync signal. These signals are known as $D_{out}$, $D_{in}$, DCL, and FSC.

The clock determines the rate of exchange of data in both the transmit and receive directions. The frame sync signal indicates when this exchange will start.

## 6.2 GCI FRAME STRUCTURE

In a GCI channel, information is in a 4–byte time–division based structure with a repetition rate of 8 kHz. The four bytes are B1 and B2 channels, a monitor (M) channel, and a C/I channel.

The two independent B channels are used to carry subscriber voice and data information. The M channel is used for operation and maintenance facilities. The C/I channel is further subdivided into two bits for the D channel information, four bits for the control/indication (C/I) channel, and two bits for the A and E channels that are used to control the transfer of information on the Monitor channel.

Figure 6–1 shows the relative positions of these channels.

## 6.3 ENABLING THE GCI MODES

GCI modes can be enabled via two different methods, depending on the application requirements.

1. The GCI mode can be enabled through the GCI control register present in the SCP. This is called indirect mode. See descriptions for OR6(2) and OR5.
2. Alternatively, if the SCP port is not required or available, then the GCI mode can be enabled at hardware reset. This is called direct mode. This is done by connecting $\overline{SCPEN}/\overline{GCIEN}$ to $V_{SS}$ during reset.

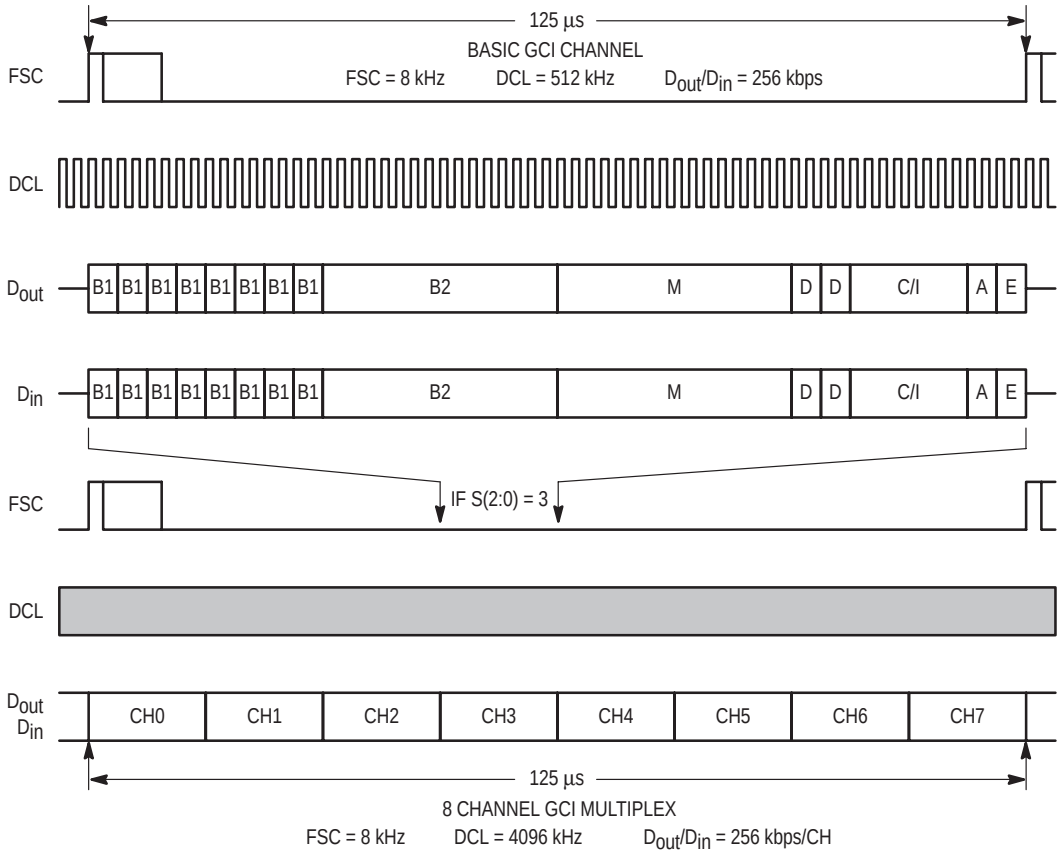



**Figure 6–1a. Relative Channel Positions (GCI Slave Mode)**

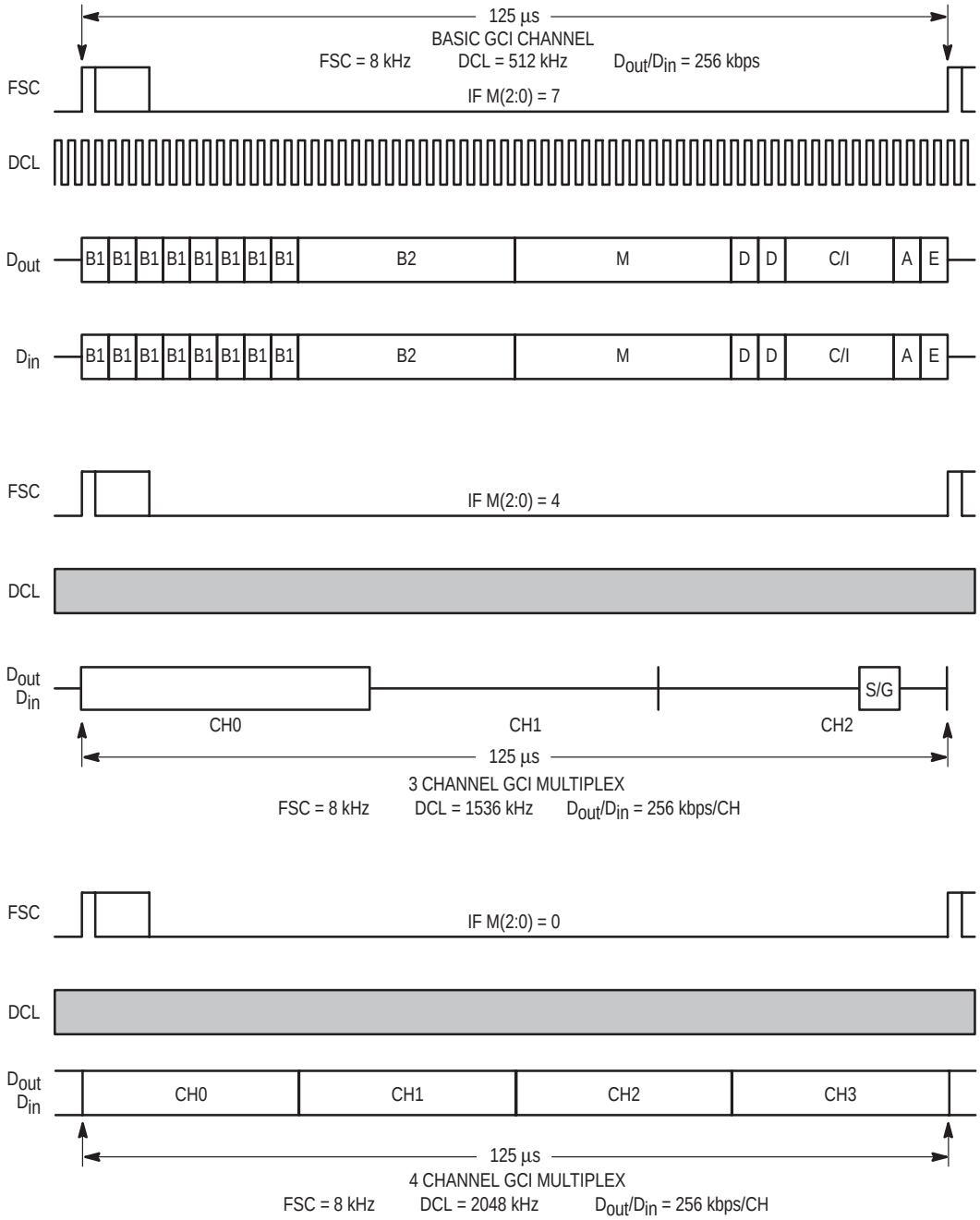



**Figure 6–1b. Relative Channel Positions (GCI Master Mode)**

## 6.4 GCI INDIRECT MODE

When control of the SCP interface is available, a pseudo GCI mode can be activated through the GCI control register. In the indirect mode, the SCP interface operates as normal and the IDL2 interface operates in a GCI type 2B+D data format mode. This means that the 2B+D data is assembled in a pseudo GCI frame for transmission, but the C/I, monitor, and A/E fields are high impedance. For reception, data is recognized in the B and D channels but is ignored in the C/I, M, and A/E channels. The SCP interface is available as normal.

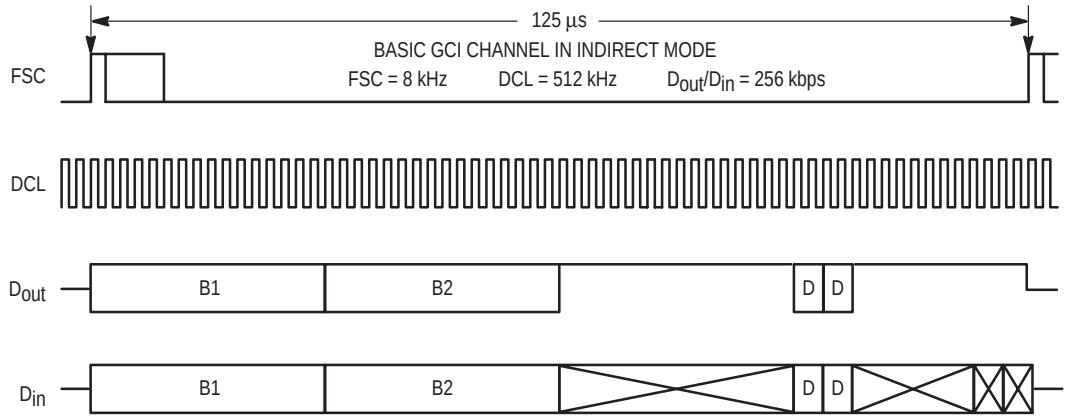



**Figure 6–2. GCI Indirect Mode**

The following GCI control bits are located in the overlay register set, in OR5 and OR6.

**GCI_IND EN, OR6(b2)**

At reset, this bit is set to a logic zero; the inactive state (i.e., normal IDL2 mode). When set to a logic one, the IDL2 port is reconfigured to have the same 2B+D data format as a GCI interface. When GCI indirect mode is inactive, OR5(2:0) and OR6(1:0) bits are disabled.

**CLK(1:0), OR6(b1, b0)**

In master mode, these two bits control the output clock frequency of GCI_DCL. CLK(1:0)=0 is the default state.

**Table 6–1. CLK1, CLK0**
**GCI Clock Selection**

| CLK1 OR6(b1) | CLK0 OR6(b0) | GCI_DCL |
|---|---|---|
| 0 | 0 | 2.048 MHz |
| 0 | 1 | 2.048 MHz |
| 1 | 0 | 1.536 MHz |
| 1 | 1 | 512 kHz |

**S(2:0), OR5(b2, b1, b0)**

These three bits select the GCI timeslot that the device will use. S(2:0)=0 is the default state, timeslot 0. The timeslot selected must be compatible with the DCL clock rate being used (i.e., if the clock rate is 2048 kHz, only the first four timeslots are available).

**Table 6–2. GCI Timeslot Assignment**

| S2 OR5(b2) | S1 OR5(b1) | S0 OR5(b0) | Timeslot |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 2 |
| 0 | 1 | 1 | 3 |
| 1 | 0 | 0 | 4 |
| 1 | 0 | 1 | 5 |
| 1 | 1 | 0 | 6 |
| 1 | 1 | 1 | 7 |

**FSC**

This is an input/output pin to which all serial interface events are synchronized. This pin is periodic at 8 kHz/125 µs. In the master mode, the pin is an output and is either derived from the S/T frame or from XTAL. In the slave mode, the pin is an input.

**DCL**

This is an input/output pin that provides the clock to the serial interface. In the master mode, this pin is an output; and in the slave mode, it is an input. The clock is continuous and is synchronous with the frame sync. The clock rate for GCI is double the bit rate (i.e., two clocks per data bit).

When programmed as an input, the clock rate can be any multiple of 16 kHz between 512 and 4096 kHz.

When programmed as an output, the clock rate can be selected via the SCP GCI control register to be either 2048, 1536, or 512 kHz.

**$D_{in}$**

This pin is always an input. Data to be output on the S/T–interface is input on this pin during the programmed timeslots. This pin is also the input for the monitor and C/I channels of the GCI frame.

**$D_{out}$**

This pin is an open drain output and requires an external pull–up resistor. This output can be wire–OR'd with other GCI devices. Data received on the S/T–interface is output on this pin during the programmed timeslot and is high impedance at all other times. This pin is also the output for the monitor and C/I channels of the GCI frame.

## 6.5 GCI DIRECT MODE

The alternative GCI mode is direct mode. This mode should be used when a fully–compliant GCI is required. In this mode, the SCP interface is not available.

In a GCI direct mode the monitor, C/I, and A/E channels are fully active and compatible with the GCI standards.

To enter a GCI direct mode, the $\overline{\text{SCPEN}}$/$\overline{\text{GCIEN}}$ pin should be tied to $V_{SS}$ and a reset applied to the device. The GCI direct mode is selected on the rising edge of $\overline{\text{RESET}}$. The $\overline{\text{GCIEN}}$ pin must be tied to $V_{SS}$ at all times when GCI direct mode is the required mode of operation. The $\overline{\text{GCIEN}}$ pin is continuously sampled internally. A “zero–to–one” transition on $\overline{\text{GCIEN}}$ will cause the MC145574 to exit from a GCI direct mode into IDL/SCP mode.

In GCI direct mode, the $\overline{\text{IRQ}}$ function is not required and is internally disabled.

On entering GCI direct mode, the pins of the MC145574 are redefined as follows.

$\overline{\text{SCPEN}}$ changes to $\overline{\text{GCIEN}}$ (an input).

FST changes to BCL (an output).

SCPCLK changes to S2 (an input) in slave mode, and M2 (an input) in master mode.

SCP Rx changes to S1 (an input) in slave mode, and M1 (an input) in master mode.

SCP Tx changes to S0 (an input) in slave mode, and M0 (an input) in master mode.

DGRANT changes to SG (an output) in TE master mode.

BCL is enabled in both the slave and master mode. BCL is an output clock which is the DCL clock divided by two. BCL is synchronous with FSC and can be used by non–GCI devices which require a locked bit frequency clock to access the B and D channel slots (i.e., codec).

### 6.5.1 Slave Mode

In the slave mode, DCL and FSC are inputs. DCL can be any frequency between 512 kHz and 4.096 MHz. In the slave mode, S2, S1, and S0 pins control the timeslot in which the device operates.

In the NT slave mode, it is possible to select both NT1 Star and NT Terminal modes via the Monitor channel. The associated pins used in the default IDL2 mode are enabled and operate in the same manner.

In the TE slave mode, the TFSC/TCLK pin is enabled and it is possible to select the TCLK and its frequency via the Monitor channel.

### 6.5.2 Master Mode

In the master mode, DCL and FSC are outputs. The M2, M1, and M0 pins control mode selection in master mode; however, these modes are defined differently for the NT and TE master.

**Table 6–3. M2, M1, and M0 Pins in GCI NT Master Mode**

| M2 | M1 | M0 | GCI NT Master Mode |
|---|---|---|---|
| 0 | 0 | 0 | DCL = 2.048 MHz, Channel 0 |
| 0 | 0 | 1 | DCL = 2.048 MHz, Channel 1 |
| 0 | 1 | 0 | DCL = 2.048 MHz, Channel 2 |
| 0 | 1 | 1 | DCL = 2.048 MHz, Channel 3 |
| 1 | 0 | 0 | DCL = 1.536 MHz, Channel 0 |
| 1 | 0 | 1 | DCL = 1.536 MHz, Channel 1 |
| 1 | 1 | 0 | DCL = 1.536 MHz, Channel 2 |
| 1 | 1 | 1 | DCL = 512 kHz, Channel 0 |

In the GCI NT master mode, it is possible to select both NT1 Star and NT Terminal modes via the Monitor channel. The associated pins used in the default IDL2 mode are enabled and operate in the same manner.

**Table 6–4. M2, M1, and M0 Pins in GCI TE Master Mode**

| M2 | M1 | M0 | GCI TE Master Mode |
|---|---|---|---|
| 0 | 0 | 0 | DCL = 2.048 MHz |
| 0 | 0 | 1 | Reserved |
| 0 | 1 | 0 | Reserved |
| 0 | 1 | 1 | Reserved |
| 1 | 0 | 0 | DCL = 1.536 MHz, Terminal Mode |
| 1 | 0 | 1 | Reserved |
| 1 | 1 | 0 | Reserved |
| 1 | 1 | 1 | DCL = 512 kHz |

In the GCI TE master mode, only three modes of operation are available.

When M(2:0) = 4, terminal mode is selected. In this mode, the MC145574 always operates in channel 0, and D channel availability is indicated in two ways:

1. If pin SG = 1, then the D channel is currently idle and available for access. If pin SG = 0, then the D channel on the passive bus is being used by another TE device.

   If the SG pin toggles during the time when the device is using the D channel, then a collision has occurred and the device stops its D channel access. SG indicates stop/go for D channel access.

2. In parallel with the SG pin, this signal is also output from the device in bit 4 of the C/I channel of CH2. This is compatible with the SCIT bus specification and is also compatible with the MC68302. This is enabled via the Monitor channel in register OR7(6).

   When M(2:0) = 7, only one GCI channel is available, and D channel availability is indicated by the SG pin only.

   The D channel access circuitry can be disabled by writing to a control register via the Monitor channel, BR7(6). When this is done, it is assumed that the device is not operating in a passive bus application and has sole use of the D channel. When disabled, the SG pin and bit always equal one, and the GCI D channel data flows transparently to the S/T loop interface.

## 6.6 2B+D CHANNELS

In the activated state, GCI transparently transmits the information in the B and D channels in the NT and TE slave modes. In TE master mode, D channel flow control is operational and access to the D channel must be requested. Refer to the section on GCI D channel operation for further details.

## 6.7 M AND A/E CHANNELS

The GCI M (or Monitor) channel is intended to be used for the transfer of operation and maintenance information between management and layer 1 entities. For the MC145574, this means that the Monitor channel is used to access the internal registers defined for the SCP mode of operation. The A/E channel is used to control the transfer of the information on the Monitor channel by providing a handshake facility.

### 6.7.1 Monitor Channel Operation

The Monitor channel is used to access the internal registers of the MC145574. All Monitor channel messages are two bytes in length. Each byte is sent twice to permit the receiving GCI device to verify data integrity. In ISDN applications, the Monitor channel is used for access to the S interface maintenance messages. The entire register set of the MC145574 can be accessed via the Monitor channel. The A and E bits in the GCI channel are used to control and acknowledge Monitor channel transfers between the MC145574 and another GCI device. When the Monitor channel is inactive, the A and E bit times from $D_{out}$ are both high impedance. The A and E bits are active when they are driven to $V_{SS}$ during their respective bit times. Pull–up resistors are required on $D_{in}$ and $D_{out}$. The E bit indicates the transmission of a new Monitor channel byte. The A bit from the opposite direction is used to acknowledge the Monitor channel byte transfer.

An idle Monitor channel is indicated by both A and E bits being inactive for two consecutive GCI frames. The A and E bits are high impedance when inactive. The Monitor channel data is $FF.

The originating GCI device transmits a byte onto the Monitor channel after receiving the A and E bits equal to 1 for at least two consecutive GCI frames. The originating GCI device also sets its outgoing E bit to 0 in the same GCI frame as the byte that is transmitted. The transmitted byte is repeated for at least two GCI frames, or is repeated in subsequent GCI frames until the MC145574 acknowledges receiving two consecutive GCI frames containing the same byte.

Once the MC145574 acknowledges the first byte, the sending device sets E to high impedance and transmits the first frame of the second byte. Then the second byte is repeated with the E bit low until it is acknowledged. See Figure 6–3 for details of Monitor channel procedure.

The destination GCI device verifies that it has received the first byte by setting the A bit to 0 towards the originating GCI device for at least two GCI frames. Successive bytes are acknowledged by the receiving device setting A to high impedance on the first instance of the next byte followed by A being cleared to 0 when the second instance of the bit is received.

If the GCI device does not receive the same Monitor channel byte in two consecutive GCI frames, it indicates this by leaving A = 0 until two consecutive identical bytes are received. The last byte of the sequence is indicated by the originating GCI device setting its E bit to 1 for two successive GCI frames.

## 6.8 MONITOR CHANNEL MESSAGES

The MC145574 supports three basic types of Monitor channel messages. The first group of messages are commands that read or write the internal register set of the MC145574. See Sections 8, 9, and 10 for the complete description of the MC145574 register set. The second group of messages are responses from the MC145574. These responses are transmitted by the MC145574 after it receives a register read or write command over the Monitor channel. The third type of Monitor channel message is the Status Indication Message. When enabled, this message indicates a change in interrupt status register NR3.

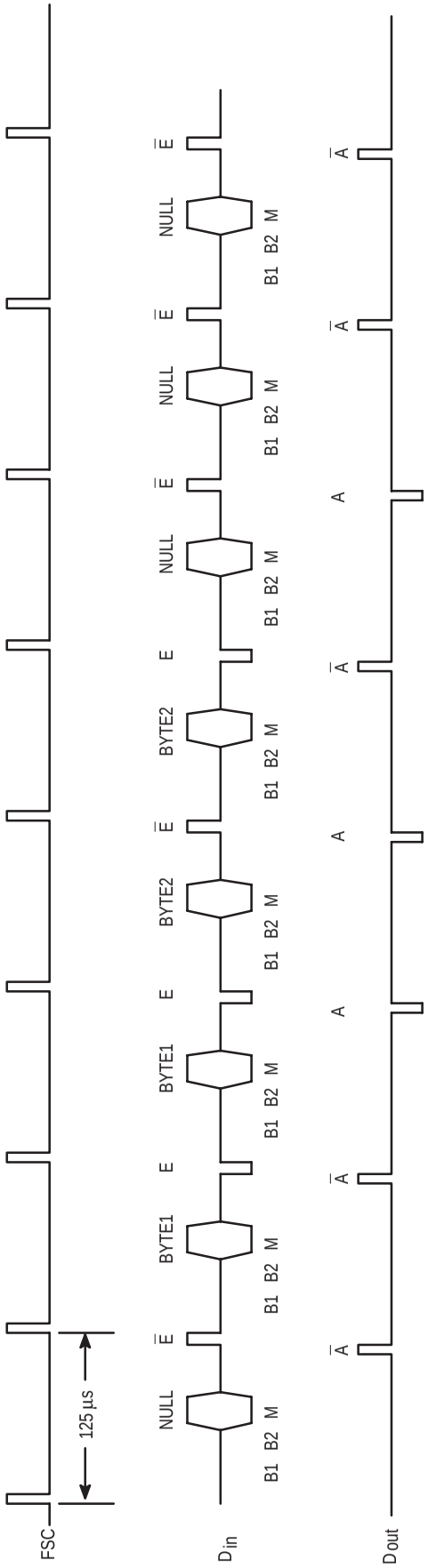



**Figure 6–3. Monitor Channel Access Protocol**

### 6.8.1 Monitor Channel Commands

A GCI device transmits Monitor channel commands to a receiving MC145574 to access its internal register set. The receiving MC145574 then transmits a Monitor channel response message onto the Monitor channel for commands that request data to be read from an internal register. Commands that write data to an internal MC145574 register are accepted and acted upon, but the MC145574 does not issue a response message. The Monitor channel commands are given in Table 6–5.

The MC145574 acknowledges all messages it receives over the Monitor channel. If an invalid message is received, the MC145574 acknowledges it but does not take any action.

**Table 6–5. Monitor Channel Commands**

| MSB | | | | Byte 1 | | | LSB | MSB | | | | Byte 2 | | | LSB | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** | **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** | **Comment** |
| 0 | 0 | 0 | 0 | ba3 | ba2 | ba1 | ba0 | d7 | d6 | d5 | d4 | d3 | d2 | d1 | d0 | Byte Write |
| 0 | 0 | 0 | 1 | ba3 | ba2 | ba1 | ba0 | X | X | X | X | X | X | X | X | Byte Read |
| 0 | 0 | 1 | 0 | 0 | na2 | na1 | na0 | d3 | d2 | d1 | d0 | X | X | X | X | Nibble Write |
| 0 | 0 | 1 | 1 | 0 | na2 | na1 | na0 | X | X | X | X | X | X | X | X | Nibble Read |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | X | X | X | X | X | X | X | X | ID Command |

### 6.8.2 Monitor Channel Response Messages

The Monitor channel response messages are transmitted onto the GCI Monitor channel by the MC145574 in response to a register read command. The Monitor channel response messages are given in Table 6–6.

**Table 6–6. Monitor Channel Response Messages**

| MSB | | | | Byte 1 | | | LSB | MSB | | | | Byte 2 | | | LSB | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** | **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** | **Comment** |
| 0 | 0 | 0 | 1 | ba3 | ba2 | ba1 | ba0 | d7 | d6 | d5 | d4 | d3 | d2 | d1 | d0 | Byte Read |
| 0 | 0 | 1 | 1 | 0 | na2 | na1 | na0 | d3 | d2 | d1 | d0 | x | x | x | x | Nibble Read |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | x | x | x | x | x | x | x | x | ID Response |

### 6.8.3 Monitor Channel Status Indication Messages

This message is automatically transmitted onto the GCI Monitor channel by the MC145574 when a status change has occurred within the device. This message is analogous to the interrupt in SCP mode. The Monitor channel status indication message is given in Table 6–7.

The status indication message is in effect a read of the interrupt status register NR3. By default, this indication message is disabled. The indication message must be first enabled by writing to the Monitor channel register NR4.

**Table 6–7. Monitor Channel Status Indication Messages**

| MSB | | | | Byte 1 | | | LSB | MSB | | | | Byte 2 | | | LSB | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** | **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** | **Comment** |
| 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | d3 | d2 | d1 | d0 | x | x | x | x | NR3 Read |

## 6.8.4 Accessible Monitor Channel Registers

The following register maps indicate the internal SCP registers that are accessible via the Monitor channel. Items that are in **bold** print indicate functions that are different to those of the SCP version. See Sections 8, 9, and 10 for initial register values after a reset.

| | | (3) | (2) | (1) | (0) |
|---|---|---|---|---|---|
| **NR1** | **NT** | Activation Indication | Error Indication | Not Applicable | Frame Sync |
| | **TE** | Activation Indication | Error Indication | Multiframing Detection | Frame Sync |
| **NR2** | | | Transmit Power Down | | Return to Normal |
| **NR3** | **NT** | IRQ3 Δ Rx Info | IRQ2 Multiframe Reception | IRQ6 FECV Detect | IRQ7 NT Term. D Ch. Coll. |
| | **TE** | IRQ3 Δ Rx Info | IRQ2 Multiframe Reception | IRQ1 D Channel Collision | Not Applicable |
| **NR4** | **NT** | IRQ3 Enable | IRQ2 Enable | IRQ6 Enable | IRQ7 Enable |
| | **TE** | IRQ3 Enable | IRQ2 Enable | IRQ1 Enable | Not Applicable |
| **NR5** | **NT** | Idle B1 Channel | Idle B2 Channel | Invert B1 Channel | Invert B2 Channel |
| | **TE** | **Enable B1 Channel** | **Enable B2 Channel** | Invert B1 Channel | Invert B2 Channel |
| **NR6** | | 2B+D GCI Transparent Loopback | | | Swap B1 and B2 |

| | | (7) | (6) | (5) | (4) | (3) | (2) | (1) | (0) |
|---|---|---|---|---|---|---|---|---|---|
| **BR2** | **NT** | SC1.1 | SC1.2 | SC1.3 | SC1.4 | | | | |
| | **TE** | Q.1 | Q.2 | Q.3 | Q.4 | | | | |
| **BR3** | **NT** | Q.1 | Q.2 | Q.3 | Q.4 | Q Qual | Int. Every Multiframe | | |
| | **TE** | SC1.1 | SC1.2 | SC1.3 | SC1.4 | Not Applicable | Int. Every Multiframe | | |
| **BR4** | | FV7 | FV6 | FV5 | FV4 | FV3 | FV2 | FV1 | FV0 |
| **BR5** | | BPV7 | BPV6 | BPV5 | BPV4 | BPV3 | BPV2 | BPV1 | BPV0 |
| **BR6** | | B1 S/T Loopback Transparent | B1 S/T Loopback Non–Transparent | B2 S/T Loopback Transparent | B2 S/T Loopback Non–Transparent | GCI B1 Loopback Transparent | GCI B1 Loopback Non–Transparent | GCI B2 Loopback Transparent | GCI B2 Loopback Non–Transparent |
| **BR7** | **NT** | Activation Procedures Disabled | Active Only NT Enable | Enable Multiframing | Invert E Channel | | | LAPD Polarity Control | Activation Timer #2 Expired |
| | **TE** | Activation Procedures Disabled | D Channel Procedures Ignored | | Map E to D | GCI Free Run | | LAPD Polarity Control | |
| **BR9** | **NT** | TXSC2.1 | TXSC2.2 | TXSC2.3 | TXSC2.4 | TXSC3.1 | TXSC3.2 | TXSC3.3 | TXSC3.4 |
| | **TE** | RXSC2.1 | RXSC2.2 | RXSC2.3 | RXSC2.4 | RXSC3.1 | RXSC3.2 | RXSC3.3 | RXSC3.4 |
| **BR10** | **NT** | TXSC4.1 | TXSC4.2 | TXSC4.3 | TXSC4.4 | TXSC5.1 | TXSC5.2 | TXSC5.3 | TXSC5.4 |
| | **TE** | RXSC4.1 | RXSC4.2 | RXSC4.3 | RXSC4.4 | RXSC5.1 | RXSC5.2 | RXSC5.3 | RXSC5.4 |
| **BR11** | | | | Rx INFO State B1 | Rx INFO State B0 | Tx INFO State B1 | Tx INFO State B0 | Ext. S/T Loopback | Transmit 96 kHz Test Signal |
| **BR12** | | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved |
| **BR13** | **NT** | NT1 Star Mode | | | Mute B2 on GCI Tx | Mute B1 on GCI Tx | Force Echo Channel to 0 | | |
| | **TE** | | | | Mute B2 on GCI Tx | Mute B1 on GCI Tx | | Force GCI Tx | |
| **BR14** | | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved |

| | | (7) | (6) | (5) | (4) | (3) | (2) | (1) | (0) |
|---|---|---|---|---|---|---|---|---|---|
| **BR15** | | Overlay Register Enabled | | Rev 5 | Rev 4 | Rev 3 | Rev 2 | Rev 1 | Rev 0 |

| | | (7) | (6) | (5) | (4) | (3) | (2) | (1) | (0) |
|---|---|---|---|---|---|---|---|---|---|
| **OR6** | | TSA B1 Enable | TSA B2 Enable | TSA D Enable | | $D_{out}$ Open Drain | GCI Indirect Mode Enable | CLK1 | CLK0 |
| **OR7** | | Disable 3 V Regulator | **Enable S/G Bit** | Enable TCLK | | | | Enable BCL | |
| **OR8** | | | | Disable XTAL | | | FIX Enable | NT Terminal Mode Enable | **Sleep Disable** |
| **OR9** | **NT** | | | | | | Force INFO 2 Transmission | | |
| | **TE** | | | | | | | T3F8 Enable | T3F6 Disable |
| **OR15** | | Overlay Register Enable | | Rev 5 | Rev 4 | Rev 3 | Rev 2 | Rev 1 | Rev 0 |

All these registers are detailed in the following sections of this document: Section 8 for the nibble registers, Section 9 for the byte registers, and Section 10 for the overlay registers.

### 6.8.5 SCP/GCI Register Differences

When configured for GCI direct mode of operation, the following register bits have different functionality from SCP mode.

**OR7(6) Enable S/G Bit**

This bit can be enabled only in GCI 1.536 MHz clock mode. This bit provides the availability of the D channel on the S/T loop. “1” = Stop (no availability of the D channel) and “0” = Go (availability of the D channel). Refer to Section 11.

**OR8(0) Sleep Disable**

In GCI mode, the sleep mode is enabled by default. It can be disabled by writing to the register bit (i.e., by writing a logic 1). This is opposite to operation of these bits in the SCP mode.

## 6.9 COMMAND INDICATE CHANNEL OPERATION

The command/indication (C/I) is intended to manage layer 1 procedures such as activation and deactivation of the line, test loop control, and other additional control functions. C/I codes are four bits in length and must be received for two consecutive GCI frames before they are acted upon.

The C/I channel bits are numbered bit 4 through bit 1, with bit 4 being the most significant bit. The C/I channel command bits are transmitted starting with bit 4.

The command channel (COM) is an input to the device in the C/I channel of the GCI frame on the $D_{in}$ pin.

The indicate channel (IND) is an output from the device in the GCI channel of the GCI frame on the $D_{out}$ pin.

In both the COM and IND cases, the four–bit word is continually input or output until superceded by another C/I channel word.

The command and indicate words used by the MC145574 device are defined in Table 6–8. This table is fully compatible with the industry standard GCI specification.

## Table 6–8. C/I Channel Commands and Indications

| C/I Code | TE Master | | TE Slave | | NT | | NT Terminal | |
|---|---|---|---|---|---|---|---|---|
| | Indication | Command | Indication | Command | Indication | Command | Indication | Command |
| 0000 | DR | TIM | DR | — | — | DR | — | DR |
| 0001 | — | RES | — | RES | — | RES | — | RES |
| 0010 | — | — | — | — | — | — | — | — |
| 0011 | — | — | — | — | — | — | — | — |
| 0100 | RSY | — | RSY | — | RSY | — | RSY | — |
| 0101 | — | — | — | — | — | — | — | — |
| 0110 | — | T1/T3EXP | — | T1/T3EXP | — | T1/T3EXP | — | T1/T3EXP |
| 0111 | — | — | — | — | — | — | — | — |
| 1000 | AR | AR8 | AR | AR | AR | AR | AR | AR8 |
| 1001 | — | AR10 | — | AR | — | AR | — | AR10 |
| 1010 | — | ARL | — | ARL | — | ARL | — | ARL |
| 1011 | — | AREOM | — | AR | — | AR | — | AREOM |
| 1100 | AI8 | — | AI | — | AI | AI | AI8 | AI |
| 1101 | AI10 | — | — | — | — | — | AI10 | — |
| 1110 | — | — | — | — | — | AIL | — | AIL |
| 1111 | DC | DI | DC | DI | DI | DC | DI | DC |

Table 6–9 lists the GCI C/I codes used, with all the codes coming from the GCI specification except for T1/T3EXP and AREOM.

## Table 6–9. GCI C/I Codes

| Command/Indication | Abbreviation |
|---|---|
| Activation Indication | AI |
| Activation Indication Priority 1 | AI8 |
| Activation Indication Priority 2 | AI10 |
| Activation Indication Local Test Loop | AIL |
| Activation Request | AR |
| Activation Request Priority 1 | AR8 |
| Activation Request Priority 2 | AR10 |
| Activation Request Local Test Loop | ARL |
| Activation Request, End of Message | AREOM |
| Deactivation Confirmation | DC |
| Deactivation Indication | DI |
| Deactivation Request | DR |
| Reset | RES |
| Resynchronization (Loss of Framing) | RSY |
| Timing Request | TIM |
| Activation Timer Expired — Force Deactivation | T1/T3EXP |

## 6.10 GCI ACTIVATION AND DEACTIVATION TIMING DIAGRAMS

The following diagrams (Figures 6–4 through 6–6) indicate the flow of the activation/deactivation procedure and are not intended to be exhaustive in all the possible permutations.

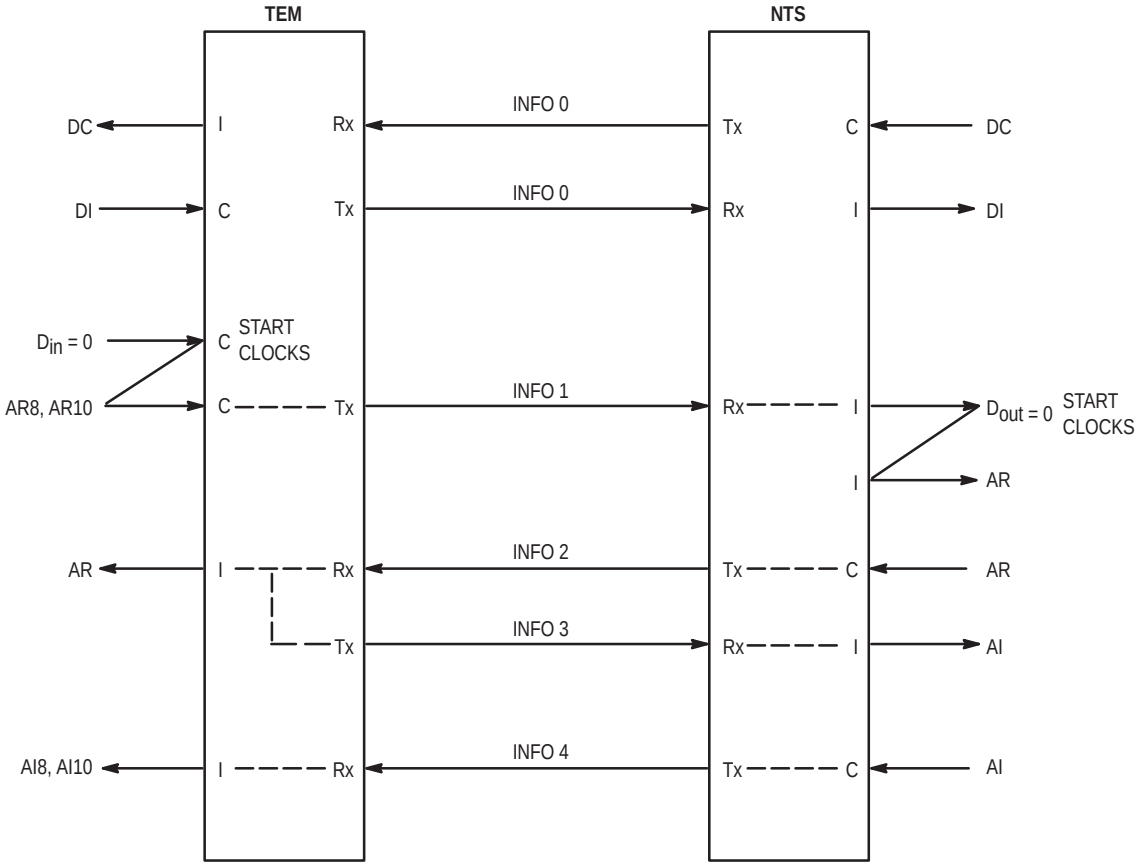



**Figure 6–4. Activation from TE End**

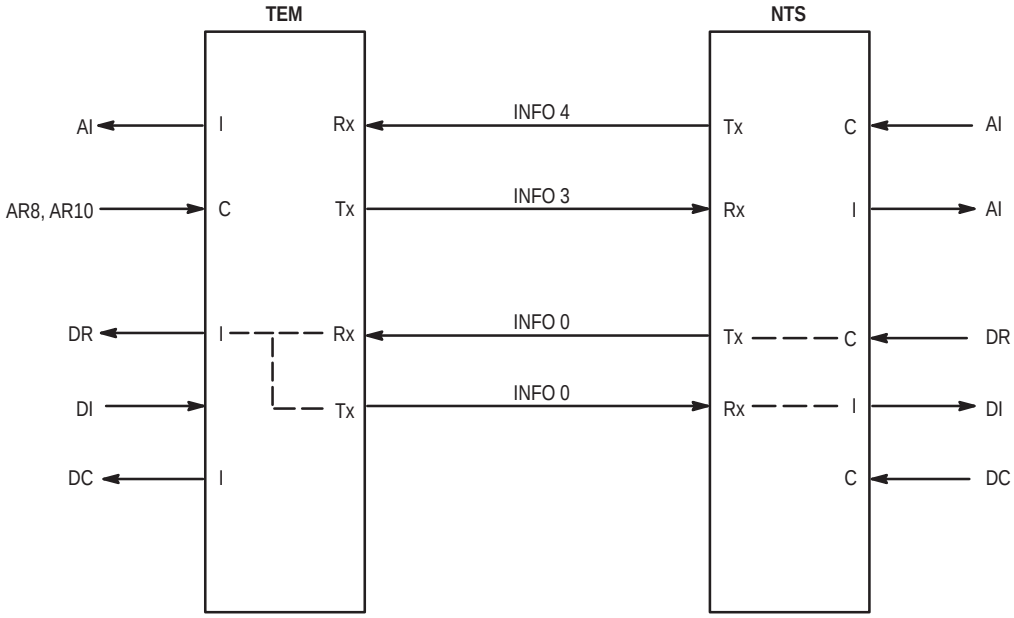



**Figure 6–5. Deactivation from NT End**

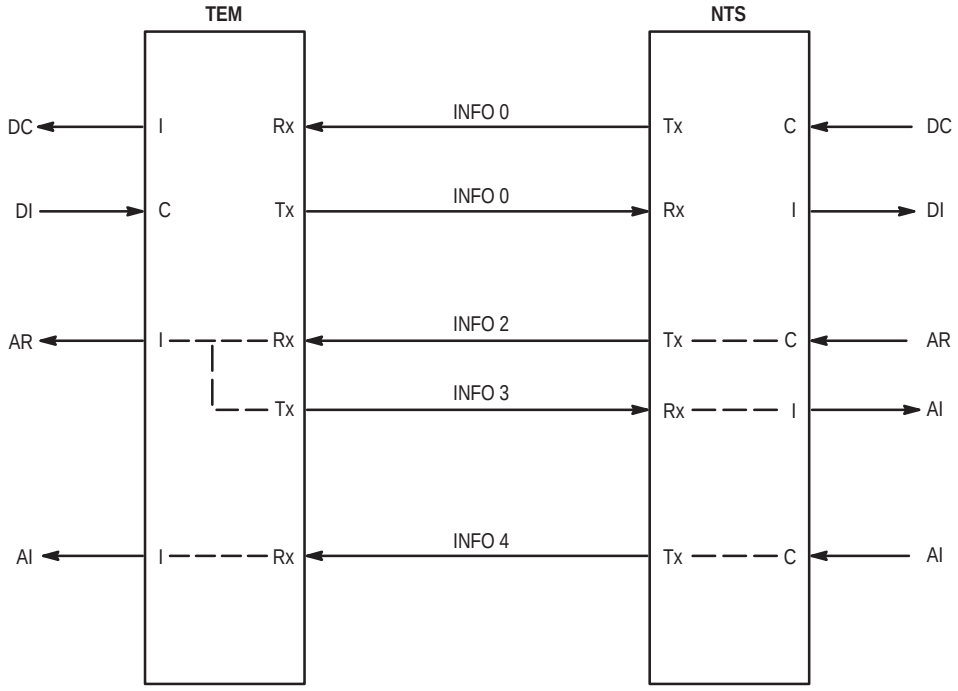



**Figure 6–6. Activation from NT End**

# 7
# PIN DESCRIPTIONS

## 7.1 INTRODUCTION

The Motorola MC145574 ISDN S/T transceiver is available in a 28–pin SOIC and a 32–pin TQFP package (see Figure 7–1).

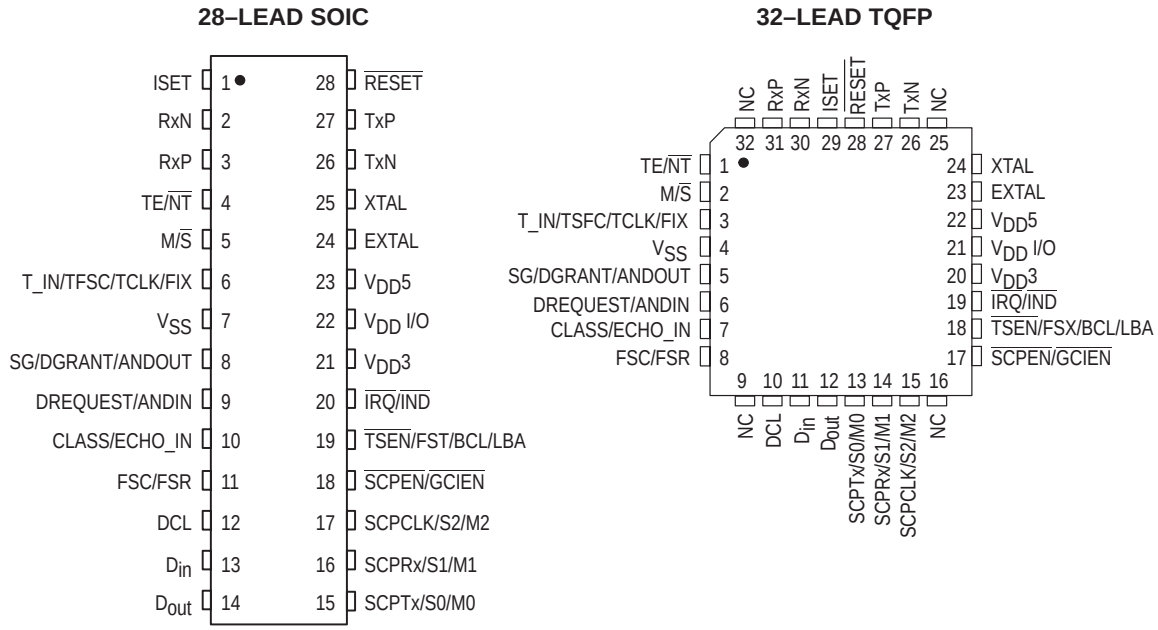



**Figure 7–1. Pin Assignments**

## 7.2 PIN DESCRIPTIONS

The following pin descriptions are not intended to be exhaustive but merely indicate the operational modes of the pins. For complete operational details please refer to the appropriate sections of this document.

### 7.2.1 ISET

In both the NT and TE modes of operation, a current programming reference resistor of value 30 kΩ accurate to 5% should be connected between this pin and $V_{SS}$. This resistor provides biasing and programs the current limit for the TxP and TxN driver circuit. Note that this resistor is not user programmable and must be 30 kΩ for CCITT 1.430, ETSI ETS 300012, and ANSI T1.605 compatibility.

### 7.2.2 RxN, RxP

These two pins form the differential receiver for the S/T–interface. They are connected to the S/T loop via a transformer. For further information, refer to Section 16.

### 7.2.3 TE/$\overline{\text{NT}}$

This pin allows the external selection of NT or TE mode. When this pin is held low, the NT mode is selected; and when it is held high, the TE mode is selected. This pin is OR'd with an SCP register bit, enabling TE/$\overline{\text{NT}}$ selection to be made in the software. This pin must be tied low to allow software selection of TE or NT mode.

### 7.2.4 M/$\overline{\text{S}}$

This pin allows the external selection of master or slave timing mode for the IDL2/GCI interface. This pin functions in both NT and TE modes. When this pin is held low, the slave mode is selected; and when it is held high, the master mode is selected. In the slave mode FSC/DCL are inputs; in the master mode FSC/DCL are outputs.

This pin is OR'd with an SCP register bit, enabling master/slave selection to be made in the software. This pin must be tied low to allow software selection of master or slave mode.

### 7.2.5 T_IN/TFSC/TCLK/FIX

This pin performs four functions dependent on the mode of operation. In all NT modes, except NT Terminal mode, this pin is the FIX input and enables the device to differentiate between fixed and adaptive timing modes. When this pin is held low, adaptive timing is selected, and when it is held high fixed timing is selected. This pin is OR'd with an SCP register bit, enabling fixed/adaptive selection to be made in the software.

In the NT Terminal mode, this pin is the T_IN input; T_IN is an IDL2 input port that accepts B1, B2, and D channel data. Refer to the NT Terminal section for further details. In the NT Terminal mode, the FIX function is controlled via an SCP register bit.

In the TE slave mode, this pin outputs TFSC. TFSC is an 8 kHz frame clock that is synchronized to the received S/T–interface and can be used as the synchronization source in the NT2 slave–slave mode.

Alternatively, this pin can output TCLK, selected via the SCP. TCLK is a clock, whose frequency can be chosen via the SCP, which is synchronized to the received S/T–interface. TCLK can be used as an alternative to TFSC in NT2 slave–slave mode.

In the TE master mode, this pin has no function and is a high–impedance output.

### 7.2.6 $V_{SS}$

This is the most negative power supply and digital logic ground. It is normally 0 V.

### 7.2.7 SG/DGRANT/ANDOUT

This pin performs three functions dependent on the mode of operation. In the NT1 Star mode, it is the ANDOUT output function for use in NT1 Star applications. In the TE master and NT Terminal modes, this pin is the DGRANT output function used for gaining D channel access. In the GCI TE master mode, this pin is SG and indicates stop/go access to the D channel.

### 7.2.8 DREQUEST/ANDIN

This pin performs two functions dependent on the mode of operation. In the NT1 Star mode, it is the ANDIN input function for use in NT1 Star applications. In the TE master and NT Terminal modes, this pin is the DREQUEST input used for requesting D channel access. In all other modes, this input has no defined function and should be tied to $V_{SS}$.

### 7.2.9 CLASS/ECHO_IN

This pin performs two functions dependent on the mode of operation. In the NT1 Star mode, it is the ECHO_IN input function for use in NT1 Star applications. In the TE master mode, this pin is the class input used to determine the D channel access class. In all other modes, this input has no defined function and should be tied to $V_{SS}$.

### 7.2.10 FSC/FSR

This pin is bidirectional; the direction depending on whether the device is to be a timing master or a slave to the IDL2/GCI interfaces. In either case, this pin should be driven with or it generates an 8 kHz frame sync signal. This pin is also the frame sync signal for the IDL2 receive direction (FSR) when independent frame syncs have been enabled via the SCP interface.

### 7.2.11 DCL

This pin is the clock pin for the IDL2/GCI interfaces and is either an input or an output depending on whether the interface is operating as a slave or a master.

### 7.2.12 $D_{in}$

This pin is the data input pin for the GCI and IDL2 interfaces.

### 7.2.13 $D_{out}$

This pin is the data output pin for the GCI and IDL2 interfaces.

### 7.2.14 SCP Tx/S0/M0

This pin has three functions. It is the data output pin (SCP Tx) in SCP mode, a timeslot select input pin (S0) in GCI slave mode, and a mode select pin (M0) in GCI master mode.

### 7.2.15 SCP Rx/S1/M1

This pin has three functions. It is the data input pin (SCP Rx) in SCP mode, a timeslot select input pin (S1) in GCI slave mode, and a mode select pin (M1) in GCI master mode.

### 7.2.16 SCPCLK/S2/M2

This pin has three functions. It is the clock input pin (SCPCLK) in SCP mode, a timeslot select input pin (S2) in GCI slave mode, and a mode select pin (M2) in GCI master mode.

### 7.2.17 $\overline{\text{SCPEN}}/\overline{\text{GCIEN}}$

This pin has two functions. It is the SCP enable input pin ($\overline{\text{SCPEN}}$) in SCP mode, and the GCI enable input pin ($\overline{\text{GCIEN}}$) in GCI mode. Refer to the section on GCI for details on how the device enters GCI mode.

### 7.2.18 $\overline{\text{TSEN}}$/FST/BCL/LBA

This pin is initially high impedance, but can be programmed to have three separate functions. When the $\overline{\text{TSEN}}$ signal is enabled via the SCP, this pin becomes an open drain output that pulls low when data is being output from $D_{out}$. This signal can then be used to enable an external driver in applications where the IDL2 2B+D data goes off–board (PBXs, etc.).

In IDL2 mode, this pin can also be used as the 8 kHz frame sync (FST) for the transmit path. In this mode, the pin is bidirectional, the direction depending on whether the device is an IDL2 master or slave. FST only operates when dual frame sync mode has been enabled via the SCP.

In GCI mode, this pin can be an output clock (BCL). BCL is a bit rate clock that is half the frequency of the DCL clock and is synchronous with FSC. This clock can be used as the data clock for standard devices such as a codec. BCL must be enabled via the GCI Monitor channel.

Loopback active (LBA) is the default function for both the IDL2 and GCI modes. This pin is initially an output. The LBA pin is normally low but when a loopback is activated within the device, this pin will transition to a high during the time that the loopback is enabled. This pin can be redefined by writing to internal registers within the device.

### 7.2.19 $\overline{\text{IRQ}}/\overline{\text{IND}}$

This pin is an open drain output that pulls low when the device wants to inform the microprocessor that a status change has occurred. This pin returns to high impedance after clearing the interrupt condition via the SCP.

In GCI mode, this pin is $\overline{\text{GCI}}_\overline{\text{IND}}$. It is an open drain output and is driven low to indicate that GCI mode is enabled.

### 7.2.20 $V_{DD}3$

This pin is the 3 V regulated supply output used to power the internal digital circuitry. This pin requires an external smoothing capacitor to be connected to ground (100 nF).

### 7.2.21 $V_{DD}$ I/O

This is the positive supply pin for the output drivers. This pin should be connected to $V_{DD}5$, if 5 V drivers are required; or the 3 V regulator output, $V_{DD}3$, if 3 V drivers are required. For further information, refer to the section on Power Supply Strategy.

### 7.2.22 $V_{DD}5$

This is the positive supply pin and is normally 5 V $\pm$ 5%. It should have a capacitor of 100 nF connected to ground. For further information, refer to the section on Power Supply Strategy.

### 7.2.23 EXTAL

This pin is an output and should be connected to the 15.36 MHz crystal using the circuit defined in Section 14.

### 7.2.24 XTAL

This pin is an output and should be connected to the 15.36 MHz crystal using the circuit defined in Section 14, or alternatively it can be driven by an external 15.36 MHz clock source.

### 7.2.25 TxN, TxP

These two pins form a differential output driver that will connect to the S/T–interface via a transformer. For further information, refer to Section 16.

### 7.2.26 $\overline{\text{RESET}}$

This pin is always an input and is the reset pin for the device. It is active low. When this pin is held low, a hardware reset is applied and the device is held in the deactivated state. At the initial application

of power, the MC145574 should be reset. This pin is a Schmitt–trigger input and could have an external RC circuit connected to perform the power–on reset function.

## 7.3 ADDITIONAL NOTES

### 7.3.1 Input Levels

The MC145574 S/T transceiver is always TTL/CMOS level compatible on all digital input pins.

### 7.3.2 Output Levels

The MC145574 is always CMOS level compatible on all digital output pins.

### 7.3.3 SCP HIDOM

The MC145574 S/T transceiver has the capability of forcing all outputs (both analog and digital) to the high–impedance state. This feature, known as the “serial control port high–impedance digital output mode” is provided to allow “in–circuit” testing of other circuits or devices resident on the same PCB without requiring the removal of the MC145574.

The SCP HIDOM mode is entered by holding $\overline{\text{SCPEN}}$ low for a minimum of 33 consecutive rising edges of the SCPCLK while SCP Rx is high. If $\overline{\text{SCPEN}}$ goes high or if SCP Rx goes low, the device exits the SCP HIDOM mode and returns to normal operation.

# 8
# NIBBLE REGISTER MAP DEFINITION

## 8.1 INTRODUCTION

There are seven nibble registers (NR0 through NR6) in the MC145574. Control and status information reside in these nibble registers, which are accessed via the SCP. For a detailed description of access procedures, refer to Section 5. The nomenclature used in this data sheet is such that NR2(3) refers to nibble register 2, bit 3.

The MC145574 nibble register map is compatible to the MC145474/475 nibble register map, the only modification being the removal of bits NR6(2) and NR6(1), related to the IDL A/M FIFOs and the addition of bits (NR2(0), NR3(0), and NR4(0) for NT mode only).

**Table 8–1. SCP Nibble Register Map for NT Operation**

| | (3) | (2) | (1) | (0) |
|---|---|---|---|---|
| **NR0** | Software Reset | Transmit Power Down | Absolute Minimum Power | Return to Normal |
| **NR1** | Activation Indication | Error Indication | Not Applicable | Frame Sync |
| **NR2** | Activation Request | Deactivation Request | Activation Timer T1 Expired | NT Terminal Class |
| **NR3** | Change in Rx Info State IRQ3 | Multiframe Reception IRQ2 | IRQ6 FECV Detection | D Channel Collision IRQ7 NT Terminal Mode |
| **NR4** | Enable IRQ3 | Enable IRQ2 | Enable IRQ6 | Enable IRQ7 |
| **NR5** | Idle B1 Channel | Idle B2 Channel | Invert B1 Channel | Invert B2 Channel |
| **NR6** | 2B+D IDL2 Loopback | | | Swap B1 and B2 |

**Table 8–2. SCP Nibble Register Map for TE Operation**

| | (3) | (2) | (1) | (0) |
|---|---|---|---|---|
| **NR0** | Software Reset | Transmit Power–Down | Absolute Minimum Power | Return to Normal |
| **NR1** | Activation Indication | Error Indication | Multiframing Detection | Frame Sync |
| **NR2** | Activation Request | Not Applicable | Activation Timer T3 Expired | Class |
| **NR3** | Change in Rx Info State IRQ3 | Multiframe Reception IRQ2 | D Channel Collision IRQ1 | Not Applicable |
| **NR4** | Enable IRQ3 | Enable IRQ2 | Enable IRQ1 | Not Applicable |
| **NR5** | Enable B1 Channel | Enable B2 Channel | Invert B1 Channel | Invert B2 Channel |
| **NR6** | 2B+D IDL2 Loopback | | | Swap B1 and B2 |

**Table 8–3. Nibble Register Initialization After Any Reset**

| | IDL TE | IDL NT | GCI TE | GCI NT |
|---|---|---|---|---|
| **NR0** | 0 | 0 | 0 | 0 |
| **NR1** | 0 | 0 | 0 | 0 |
| **NR2** | 0 | 0 | 0 | 0 |
| **NR3** | 8 | 0 | 8 | 0 |
| **NR4** | 0 | 0 | 0 | 0 |
| **NR5** | 0 | 0 | 0 | 0 |
| **NR6** | 0 | 0 | 0 | 0 |

NOTE: All values in hexadecimal unless shown otherwise.

## 8.2 NR0

This register is a read/write register and can be reset by a hardware reset. A per–bit description of nibble register 0 (NR0) follows.

| | b3 | b2 | b1 | b0 |
|---|---|---|---|---|
| **NR0** | Software Reset<br>rw | Transmit Power–Down<br>rw | Absolute Minimum Power<br>rw | Return to Normal<br>rw |

**NR0(3) — Software Reset**

When NR0(3) is 0, the MC145574 functions normally. When this bit is set to 1, a software reset is applied to the internal circuits of the S/T transceiver. The effect of the software reset is the equivalent of holding the external reset input low (hardware reset), except that NR0(3:0) is not reset. Thus, when this bit is set, all internal registers (except NR0) are returned to their initial state. Application of either a hardware or software reset has the effect of re–initializing all the internal registers; it does not prevent access to the SCP. Note that NR0(3) is a read/write bit.

**NR0(2) — Transmit Power–Down**

When NR0(2) is 0, the S/T transceiver functions normally. When NR0(2) is set to 1, the S/T transceiver enters a power conservation mode. In this mode the transmit section of the transceiver is held in the INFO 0 state and IDL2 Tx is held in the “idle 1s” condition. When NR0(2) = 1, the receive circuitry of the transceiver is still functional, allowing an interrupt to be generated in the event of a change in state of the received signal. Note that NR0(2) is a read/write bit. This bit has no effect on the operation of the SCP. If BR13(1) is set, the S/T transceiver outputs data on $D_{out}$.

**NR0(1) — Absolute Minimum Power**

When this bit is 0, the MC145574 functions normally. When this bit is set to 1, the chip enters a power conservation mode. In this mode a software reset is applied to the chip, all circuits are initialized, all clocking of the device is blocked, and the nonessential bias to the analog functions of the transceiver are removed such that the device consumes the absolute minimum amount of power. The transmit section of the chip is held in the INFO 0 state and IDL2 Tx is held in the “idle 1s” condition. Note that NR0(1) is a read/write bit. This bit has no effect on the operation of the SCP. In this mode, only the SCP can operate.

**NR0(0) — Return to Normal**

When this bit is 0, the MC145574 functions normally. When this bit is 1, the following bits are reset:

BR11(0) 96 kHz Test Signal
BR11(1) External S/T Loopback
BR6(7:0)

Note that NR0(0) is a read/write bit.

## 8.3 NR1

This register is a read only register and can be reset by application of either a hardware or software reset. A per–bit description of nibble register 1 (NR1) follows.

| | b3 | b2 | b1 | b0 |
|---|---|---|---|---|
| **NR1** | Activation Indication<br>ro | Error Indication<br>ro | NT: Not Applicable<br>TE: Multiframing Detection<br>ro | Frame Sync<br>ro |

**NR1(3) — Activation Indication (AI)**

This bit is set by the MC145574 when the loop is fully activated. Thus, when the MC145574 is configured as an NT, this bit is set when it is transmitting INFO 4 and receiving INFO 3. Conversely, when the MC145574 is configured as a TE, this bit is set when it is transmitting INFO 3 and receiving INFO 4. Note that NR1(3) is a read only bit.

**NR1(2) — Error Indication (EI)**

NR1(2) is set by the MC145574 S/T transceiver to indicate an error condition has been detected by the activation state machine of the transceiver, as outlined in CCITT I.430, ETSI ETS 300012, and ANSI T1.605. The low–to–high level transition of the EI bit corresponds to the EI1 error indication reporting, while the high–to–low level transition of the EI bit corresponds to the EI2 error indication reporting recovery. Note that NR1(2) is a read only bit.

**NR1(1) — NT: Not Applicable**
**TE: Multiframing Detection (MD)**

In the TE mode of operation, this bit is set by the MC145574 S/T transceiver whenever it detects multiframing from the NT. This bit will be set low if multiframing synchronization is lost and will return high when synchronization is re–acquired. This bit applies only to TE–configured devices. Note that NR1(1) is a read only bit.

**NR1(0) — Frame Sync (FS)**

NR1(0) is set high by the MC145574 S/T transceiver when frame synchronization is achieved. NR1(0) is reset by the MC145574 whenever frame synchronization is lost. Note that NR1(0) is a read only bit.

## 8.4 NR2

This register is a read/write register and can be cleared by application of either a hardware or software reset. A per–bit description of nibble register 2 (NR2) is as follows.

| | b3 | b2 | b1 | b0 |
|---|---|---|---|---|
| **NR2** | Activation Request<br>rw | NT: Deactivate Request<br>TE: Not Applicable<br>rw | Activation Timer Expired<br>rw | NT: NT Terminal Class<br>TE: Class<br>rw |

**NR2(3) — Activation Request (AR)**

When NR2(3) is set to 1, an activation request input is passed to the activate state machine within the MC145574 S/T transceiver, as outlined in CCITT I.430, ETSI ETS 300012, and ANSI T1.605. If the transceiver is in the idle state (i.e., transmitting and receiving INFO 0) and is configured as an NT, then AR causes INFO 2 to be sent out on the transmit side of the S/T–interface. Alternatively, if the chip is configured as a TE and is in the idle state, then writing a 1 to NR2(3) causes INFO 1 to be sent out. Note that this bit will be returned low by the MC145574 S/T transceiver after its active

transition (low–to–high) has been recognized by the activation/deactivation state machine of the transceiver. This action indicates that the requested action has been recognized. Note that NR2(3) is a read/write bit.

**NR2(2) — NT: Deactivate Request DR**
**TE: Not Applicable**

When NR2(2) is set to 1, a deactivate request input is passed to the activation state machine within the MC145574 S/T transceiver, as outlined in CCITT I.430, ETSI ETS 300012, and ANSI T1.605. The deactivate request input is used to initiate deactivation of the transmission loop. Note that this bit will be returned low by the MC145574 S/T transceiver after its active transition (low–to–high) has been recognized by the activation/deactivation state machine of the transceiver. This action indicates that the requested action has been recognized and deactivation is proceeding. Note that NR2(2) is a read/write bit.

**NR2(1) — Activation Timer Expired Input**
**NT: Timer #1**
**TE: Timer #3**

When NR2(1) is set to 1, an activation timer expired input is passed to the activation state machine of the MC145574 S/T transceiver. If the transceiver is configured as an NT, this bit corresponds to the Timer #1 expire input. If the transceiver is configured as a TE, this bit corresponds to the Timer #3 expire input. These timers correspond to the activation timers outlined in CCITT I.430, ETSI ETS 300012, and ANSI T1.605. The timer expire input informs the activation/deactivation state machine that sufficient time has elapsed since the request to activate the loop and that attempts to do so should be abandoned. This bit is normally set by the controlling device and is automatically cleared when the MC145574 has deactivated the loop. This bit can be reset by hardware or a software reset. Note that NR2(1) is a read/write bit.

**NR2(0) — NT : NT Terminal Class**
**TE : Class**

When the MC145574 is configured for TE mode, this bit sets the class for D channel operation. When this bit is 0, the chip is set for class 1 operation. Alternatively, when this bit is 1, the chip is configured for class 2 operation. Class 1 and class 2 operations are as per CCITT I.430, ETSI ETS 300012, and ANSI T1.605 (i.e., class 1 is the higher class, used for signalling information, and class 2 is the lower class). The class can also be chosen externally by means of the CLASS/ECHO_IN pin. In this case, the class is chosen by the logical ‘OR’ of the external pin and NR2(0). NR2(0) can be reset by a hardware or a software reset. Refer to Section 11 for a detailed description of the D channel. Note that NR2(0) is a read/write bit.

In the NT Terminal mode, this bit sets the class for D channel operation idle in the TE mode.

## 8.5 NR3

This register is a read/write register and can be reset by application of either a hardware or software reset. A per–bit description of nibble register 3 (NR3) follows.

| | b3 | b2 | b1 | b0 |
|---|---|---|---|---|
| **NR3** | Change in RX INFO State IRQ3<br>rw | Multiframe Reception IRQ2<br>rw | NT: IRQ6 FECV Detection<br>TE: D Channel Collision IRQ1<br>rw | NT: IRQ7 NT Terminal D Channel Collision<br>TE: Not Applicable<br>rw |

**NR3(3) — Change in Rx INFO State IRQ3**

The interrupt request condition IRQ3 is generated whenever a change occurs in the received information state of the transceiver. In the NT mode, this corresponds to a change in the receiving INFO 0,

INFO 1, INFO 3, or INFO X state. Alternatively, in the TE mode, this corresponds to a change in the receiving INFO 0, INFO 2, INFO 4, or INFO X state. Thus, when a change occurs in one of these states, the MC145574 internally sets this bit. An external interrupt will occur if “Enable IRQ3” (NR4(3)) is set. IRQ3 can be cleared by writing a 0 to NR3(3). This bit is reset by a software or a hardware reset.

Note that the transmission states for the NT (INFO 0, INFO 2, and INFO 4) and for the TE (INFO 0, INFO 1, and INFO 3) are as defined in Section 3. INFO X is defined as any transmission state other than those states. An example of such a state would be when the MC145574 is programmed to transmit a 96 kHz test tone (BR11(0) = 1). Note that NR3(3) is a read/write bit.

An INFO X state interrupt is generated only when receive INFO X state has persisted for > 8 ms. This avoids spurious interrupts during transient INFO X changes seen during activation but allows indication of prolonged INFO X conditions.

**NR3(2) — Multiframe Reception IRQ2**

This bit is for multiframe detection indication. Multiframing is initiated by the NT by setting BR7(5). A multiframe is 20 basic frames or 5 ms in duration. If this interrupt is enabled by setting NR4(2) and if multiframing is in progress, then an interrupt will be generated on multiframe boundaries; i.e., every 5 ms. Alternatively, an NT–configured MC145574 can be programmed to generate an interrupt only in the event of a new Q channel nibble having been received. Similarly, a TE–configured MC145574 can be programmed to generate an interrupt only in the event of a new SC1 subchannel having been received. Refer to Section 12 for a detailed description of these features.

A mutiframing interrupt is cleared by reading BR3. Reading BR3 will clear the interrupt in both the NT and TE modes of operation, regardless of whether the MC145574 is configured to generate an interrupt in the event of a new nibble or every multiframe. Note that NR3(2) is a read only bit.

**NR3(1)**

**NT: IRQ6 FECV Detection** — The IRQ6 status bit is set when the NT has detected a far–end code violation. See Section 15.6 for more details.

**TE: D Channel Collision IRQ1** — NR3(1) is an interrupt bit used to indicate to external devices that a collision has occurred on the D channel. A D channel collision is considered to have occurred when the TE is transmitting on the D channel (both DREQUEST and DGRANT being high), and the received E echo bit from the NT does not match the previously modulated D bit. The interrupt condition is cleared by writing a 0 to NR3(1). This bit is maskable by means of NR4(1). Note that NR3(1) is a read/write bit.

**NR3(0) — NT: D Channel Collision IRQ7 NT Terminal Mode**
**TE: Not Applicable**

NR3(0) is an interrupt bit used to indicate to external devices that a collision has occurred on the D channel. A D channel collision is considered to have occurred when the NT is transmitting on the IDL2 Tx D channel via the T_IN input pin (both DREQUEST and DGRANT being high), and the transmitted E echo bit to the TE does not match the previously input T_IN bit. The interrupt condition is cleared by writing a 0 to NR3(0). This bit is maskable by means of NR4(0). Note that NR3(0) is a read/write bit.

## 8.6 NR4

This register is a read/write register and can be reset by application of either a hardware or software reset. A per–bit description of nibble register 4 (NR4) follows.

| | b3 | b2 | b1 | b0 |
|---|---|---|---|---|
| **NR4** | Enable IRQ3<br>rw | Enable IRQ2<br>rw | NT: Enable IRQ6<br>TE: Enable IRQ1<br>rw | NT: Enable IRQ7<br>TE: Not Applicable<br>rw |

**NR4(3) — Enable IRQ3**

NR4(3) is an interrupt mask bit for IRQ3. When this bit is set high and IRQ3 is pending (i.e., NR3(3) having been internally set to a 1), an interrupt is given to an external device by holding the IRQ* pin low. The IRQ* pin will be held low until the interrupt condition is cleared by writing a 0 to NR3(3). When the interrupt mask bit NR4(3) is a 0, NR3(3) cannot cause an interrupt to the external device. This bit can be reset by either a software or hardware reset. Note that NR4(3) is a read/write bit.

**NR4(2) — Enable IRQ2**

NR4(2) is an interrupt mask bit for IRQ2. When this bit is set high and IRQ2 is pending (i.e., NR3(2) having been internally set to a 1), an interrupt is given to an external device by holding the IRQ* pin low. The IRQ* pin will be held low until the interrupt condition is cleared by reading BR3. When the interrupt mask bit (NR4(2)) is a 0, NR3(2) cannot cause an interrupt to the external device. This bit can be reset by either a software or a hardware reset. Note that NR4(2) is a read/write bit.

**NR4(1) — NT: Enable IRQ6**
**TE: Enable IRQ1**

NR4(1) is an interrupt mask bit for IRQ1 or IRQ6. When this bit is set high and IRQ1 is pending (i.e., NR3(1) having been internally set to a 1), an interrupt is given to an external device by holding the IRQ* pin low. The IRQ* pin will be held low until the interrupt condition is cleared by writing a 0 to NR3(1). When the interrupt mask bit NR4(1) is a 0, NR3(1) cannot cause an interrupt to the external device. This bit can be reset by either a software or a hardware reset. Note that NR4(1) is a read/write bit.

**NR4(0) — NT: Enable IRQ7**
**TE: Not Applicable**

NR4(0) is an interrupt mask bit for IRQ7. When this bit is set high and IRQ7 is pending (i.e., NR3(0) having been internally set to a 1), an interrupt is given to an external device by holding the IRQ* pin low. The IRQ* pin will be held low until the interrupt condition is cleared by writing a 0 to NR3(0). When the interrupt mask bit NR4(0) is a 0, NR3(0) cannot cause an interrupt to the external device. This bit can be reset by either a software or a hardware reset. Note that NR4(0) is a read/write bit.

## 8.7 NR5

This register is a read/write register and can be reset by application of either a hardware or software reset. A per–bit description of nibble register 5 (NR5) follows.

| | b3 | b2 | b1 | b0 |
|---|---|---|---|---|
| **NR5** | NT: Idle B1 Channel<br>TE: Enable B1 Channel<br>rw | NT: Idle B2 Channel<br>TE: Enable B2 Channel<br>rw | Invert B1 Channel<br>rw | Invert B2 Channel<br>rw |

**NR5(3)**

**NT: Idle B1 Channel** — In the NT mode, NR5(3) functions as a B1 channel idle bit. When NR5(3) is 0, the MC145574 functions normally where data received in the B1 channel timeslot via the IDL2 is modulated onto the S/T–interface in the B1 channel timeslot. When NR5(3) is 1, data input on the IDL2 Rx pin in the B1 channel timeslot is ignored, and the “idle 1s” condition exists on the B1 channel timeslot on the S/T–interface. Note that the default condition (i.e., after power–up or after a reset) for NR5(3) is 0, thereby allowing the data received via the IDL2 interface to be modulated onto the transmission loop. Note that NR5(3) is a read/write bit in the NT mode.

**TE: Enable B1 Channel** — In the TE mode of operation, NR5(3) functions as a B1 channel enable bit. In the TE mode B1 channel data is forced to the “idle 1s” condition on the S/T transmission loop when NR5(3) is 0. When NR5(3) is 1 (enabled), B1 channel data input via the IDL2 interface is modulated and transmitted onto the S/T transmission loop in the B1 channel timeslot. The default condition (i.e., after power–up or after a reset) for TE mode devices forces the B1 channel bits to the “idle 1s” condition. This is to avoid B channel interference until the B channels are assigned by the network.

This function may be used in multidrop configurations or in applications where the output B channel transmission must be held in the “idle 1s” condition. Note that NR5(3) is a read/write bit in the TE mode.

**NR5(2)**

**NT: Idle B2 Channel** — In the NT mode, NR5(2) functions as a B2 channel idle bit. When NR5(2) is 0, the MC145574 functions normally, where data received in the B2 channel timeslot via the IDL2 is modulated onto the S/T transmission loop in the B2 channel timeslot. When NR5(2) is 1, data input on the IDL2 Rx pin in the B2 channel timeslot is ignored, and the “idle 1s” condition exists on the B2 channel timeslot on the S/T transmission loop. Note that the default condition (i.e., after power–up or after a reset) for NR5(2) is 0, thereby allowing the data received via the IDL2 interface to be modulated onto the transmission loop. Note that NR5(2) is a read/write bit in the NT mode.

**TE: Enable B2 Channel** — In the TE mode of operation, NR5(2) functions as a B2 channel enable bit. In the TE mode B2 channel data is forced to the “idle 1s” condition on the S/T transmission loop when NR5(2) is 0. When NR5(2) is 1 (enabled), B2 channel data input via the IDL2 interface is modulated and transmitted onto the S/T transmission loop in the B2 channel timeslot. The default condition (i.e., after power–up or after a reset) for TE mode devices forces the B2 channel bits to the “idle 1s” condition. This is to avoid B channel interference until the B channels are assigned by the network. This function may be used in multidrop configurations or in applications where the output B channel transmission must be held in the “idle 1s” condition. Note that NR5(2) is a read/write bit in the TE mode.

**NR5(1) — Invert B1 Channel**

When NR5(1) is 0, the B1 channel data received via the IDL2 interface is transmitted normally on the transmission loop. When NR5(1) is set to 1, the B1 channel data received via the IDL2 interface is inverted before entering the modulator portion of the MC145574 S/T transceiver, prior to transmission on the S/T loop in the B1 timeslot. The selected B1 channel data received via the transmission loop is also inverted before being output on the IDL2 Tx pin when this function is invoked. This feature is useful in applications where it is required to use inverted data. Note that NR5(1) is a read/write bit.

**NR5(0) — Invert B2 Channel**

When NR5(0) is 0, the B2 channel data received via the IDL2 interface is transmitted normally on the transmission loop. When NR5(0) is set, the B2 channel data received via the IDL2 interface is inverted before entering the modulator portion of the MC145574 S/T transceiver prior to transmission on the S/T loop in the B2 timeslot. The selected B2 channel data received via the transmission loop is also inverted before being output on the IDL2 Tx pin when this function is invoked. This feature is useful in applications where inverted data is required. Note that NR5(0) is a read/write bit.

## 8.8 NR6

This register is a read/write register and can be reset by application of either a hardware or software reset. A per–bit description of nibble register 6 (NR6) is as follows.

| | b3 | b2 | b1 | b0 |
|---|---|---|---|---|
| **NR6** | 2B+D IDL2 Loopback<br>rw | | | Swap B1 and B2<br>rw |

**NR6(3) – 2B+D IDL2 Loopback**

When NR6(3) is 0, the MC145574 S/T transceiver functions normally. When NR6(3) is set to 1, the B1, B2, and D channel data input on the IDL2 Rx input pin are buffered and returned to the IDL2 Tx output pin on the next IDL2 cycle. The output B1, B2, and D channel data is passed unchanged to the modulator portion of the transceiver and transmitted onto the S/T loop (i.e., the loopback is transparent). Note that NR6(3) is a read/write bit.

**NR6(0) – Swap B1 and B2**

When NR6(0) is 0, the timeslot assigned positions of the B1 and B2 channel data input and output via the IDL2 interface functions normally. When NR6(0) is set to 1, the timeslot positions of the B1 and B2 channels are reversed; i.e., data entering the device on IDL2 Rx in the B1 timeslot is modulated onto the B2 timeslot, on the S/T loop. Data demodulated from the B2 timeslot from the S/T loop is output on IDL2 Tx in the B1 timeslot. The situation is analogous for B2 data entering the device on IDL2 Rx. This feature is useful in applications where a particular device (such as a codec filter) is hard–wired to a particular IDL2 timeslot and needs to gain access to the opposite B channel timeslot. NR6(0) has no effect during a 2B+D IDL2 loopback. Note that NR6(0) is a read/write bit.

NOTE: When NR6(0) is set, the B channel used on the IDL bus must be enabled before being output on the S/T loop. For example, if data entering the device on $D_{in}$ in the B1 channel is modulated onto the B2 channel on the S/T loop, then NR5(3) has to be set. On the MC145474/75, this is done differently. For the same example, NR5(2) is set instead of NR5(3).

## 8.9 NR7

NR7 is a pointer register used when accessing a 16–byte–wide register. This pointer register will contain the address of the byte–wide register to be read from or written to, on the following SCP transaction. This nibble register is not shown on the register map, as it is not programmable.

# 9
# BYTE REGISTER MAP DESCRIPTION

## 9.1 INTRODUCTION

There are 16 byte registers (BR0 through BR15) in the MC145574. Control, status, and maintenance information reside in these byte registers, which are accessed via the SCP. For a detailed description of access procedures, refer to Section 5. The nomenclature used in this data sheet is such that BR2(3) refers to byte register 2, bit 3.

The byte register map is fully compatible with the byte register map of the MC145474, with the exception of:

1. The functions that were related to the IDL2 A/M FIFOs have been removed. Writing to these registers has no effect, and reading them returns FFH.
2. The TTL input level bit BR13(6) has been removed. The digital inputs are CMOS and TTL compatible. Writing to this bit has no effect, and reading it returns 0 or 1 depending on what value, if any, has been written.
3. The only addition to the byte register map is the bit BR15(0), used for enabling the overlay registers.

**Table 9–1. Byte Register Map for NT Mode of Operation**

| | (7) | (6) | (5) | (4) | (3) | (2) | (1) | (0) |
|---|---|---|---|---|---|---|---|---|
| **BR2** | SC1.1 | SC1.2 | SC1.3 | SC1.4 | | | | |
| **BR3** | Q.1 | Q.2 | Q.3 | Q.4 | Q Qual | Interrupt Every Multiframe | | |
| **BR4** | FV7 | FV6 | FV5 | FV4 | FV3 | FV2 | FV1 | FV0 |
| **BR5** | BPV7 | BPV6 | BPV5 | BPV4 | BPV3 | BPV2 | BPV1 | BPV0 |
| **BR6** | B1 S/T Loopback Transparent | B1 S/T Loopback Non–Transparent | B2 S/T Loopback Transparent | B2 S/T Loopback Non–Transparent | IDL2 B1 Loopback Transparent | IDL2 B1 Loopback Non–Transparent | IDL2 B2 Loopback Transparent | IDL2 B2 Loopback Non–Transparent |
| **BR7** | Activation Procedures Disabled | Active Only NT Enable | Enable Multiframing | Invert E Channel | IDL2 Master Mode | IDL2 Clock Speed (LSB) | LAPD Polarity Control | Activation Timer #2 Expired |
| **BR9** | TXSC2.1 | TXSC2.2 | TXSC2.3 | TXSC2.4 | TXSC3.1 | TXSC3.2 | TXSC3.3 | TXSC3.4 |
| **BR10** | TXSC4.1 | TXSC4.2 | TXSC4.3 | TXSC4.4 | TXSC5.1 | TXSC5.2 | TXSC5.3 | TXSC5.4 |
| **BR11** | Do Not React to INFO 1 | Do Not React to INFO 3 | Rx INFO State B1 | Rx INFO State B0 | Tx INFO State B1 | Tx INFO State B0 | External S/T Loopback | Transmit 96 kHz Test Signal |
| **BR12** | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved |
| **BR13** | NT1 Star Mode | Reserved | IDL2 Clock Speed (MSB) | Mute B2 on IDL2 Tx | Mute B1 on IDL2 Tx | Force Echo Channel to Zero | Not Applicable | Reserved |
| **BR14** | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved |
| **BR15** | Overlay Register Enabled | | Rev 5 | Rev 4 | Rev 3 | Rev 2 | Rev 1 | Rev 0 |

## Table 9–2. Byte Register Map for TE Mode of Operation

| | (7) | (6) | (5) | (4) | (3) | (2) | (1) | (0) |
|---|---|---|---|---|---|---|---|---|
| **BR2** | Q.1 | Q.2 | Q.3 | Q.4 | | | | |
| **BR3** | SC1.1 | SC1.2 | SC1.3 | SC1.4 | Not Applicable | Interrupt Every Multiframe | | |
| **BR4** | FV7 | FV6 | FV5 | FV4 | FV3 | FV2 | FV1 | FV0 |
| **BR5** | BPV7 | BPV6 | BPV5 | BPV4 | BPV3 | BPV2 | BPV1 | BPV0 |
| **BR6** | B1 S/T Loopback Transparent | B1 S/T Loopback Non–Transparent | B2 S/T Loopback Transparent | B2 S/T Loopback Non–Transparent | IDL2 B1 Loopback Transparent | IDL2 B1 Loopback Non–Transparent | IDL2 B2 Loopback Transparent | IDL2 B2 Loopback Non–Transparent |
| **BR7** | Activation Procedures Disabled | D Channel Procedures Ignored | Not Applicable | Map E to D | IDL2 Free Run | IDL2 Clock Speed (LSB) | LAPD Polarity Control | |
| **BR9** | RXSC2.1 | RXSC2.2 | RXSC2.3 | RXSC2.4 | RXSC3.1 | RXSC3.2 | RXSC3.3 | RXSC3.4 |
| **BR10** | RXSC4.1 | RXSC4.2 | RXSC4.3 | RXSC4.4 | RXSC5.1 | RXSC5.2 | RXSC5.3 | RXSC5.4 |
| **BR11** | Not Applicable | Not Applicable | Rx INFO State B1 | Rx INFO State B0 | Tx INFO State B1 | Tx INFO State B0 | External S/T Loopback | Transmit 96 kHz Test Signal |
| **BR12** | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved |
| **BR13** | Not Applicable | Reserved | IDL2 Clock Speed (MSB) | Mute B2 on IDL2 Tx | Mute B1 on IDL2 Tx | Not Applicable | Force IDL2 Tx | Reserved |
| **BR14** | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved |
| **BR15** | Overlay Register Enabled | | Rev 5 | Rev 4 | Rev 3 | Rev 2 | Rev 1 | Rev 0 |

## Table 9–3. Byte Register Initialization After Any Reset

| | IDL TE | IDL NT | GCI TE | GCI NT |
|---|---|---|---|---|
| **BR0** | FF | FF | FF | FF |
| **BR1** | FF | FF | FF | FF |
| **BR2** | F0 | 00 | F0 | 00 |
| **BR3** | 00 | F0 | 00 | F0 |
| **BR4** | 00 | 00 | 00 | 00 |
| **BR5** | 00 | 00 | 00 | 00 |
| **BR6** | 00 | 00 | 00 | 00 |
| **BR7** | 00 | 00 | 00 | 00 |
| **BR8** | 00 | 00 | 00 | 00 |
| **BR9** | 00 | 00 | 00 | 00 |
| **BR10** | 00 | 00 | 00 | 00 |
| **BR11** | 00 | 00 | 00 | 00 |
| **BR12** | 00 | 00 | 00 | 00 |
| **BR13** | 00 | 00 | 00 | 00 |
| **BR14** | 00 | 00 | 00 | 00 |
| **BR15** | 00XX XXXX | 00XX XXXX | 00XX XXXX | 00XX XXXX |

NOTES:

1. All values in hexadecimal unless shown otherwise.
2. BR15 and OR15 are the same register.
3. BR0, BR1, and BR8 are reserved registers. Do not use.

## 9.2 BR0

The functions that were related to the IDL2 M FIFO of the MC145474 have been removed; writing to this register has no effect, and reading it returns FFH. (No register shown.)

## 9.3 BR1

The functions that were related to the IDL2 A FIFO of the MC145474 have been removed; writing to this register has no effect, and reading it returns FFH. (No register shown.)

## 9.4 BR2

| | (7) | (6) | (5) | (4) | (3) | (2) | (1) | (0) |
|---|---|---|---|---|---|---|---|---|
| **BR2** | NT: SC1.1<br>TE: Q.1 | NT: SC1.2<br>TE: Q.2 | NT: SC1.3<br>TE: Q.3 | NT: SC1.4<br>TE: Q.4 | | | | |

**BR2(7:4)**

**NT: Subchannel 1 (SC1) to S/T Loop** — BR2(7:4) are used for multiframing. In the NT mode of operation, these four bits correspond to subchannel 1 for transmission to the TE(s). Multiframing is initiated by the NT by setting BR7(5). When multiframing is enabled, the NT will transmit the bits in BR2(7:4) as subchannel 1, in accordance with CCITT I.430, ETSI ETS 300012, and ANSI T1.605. BR2(7:4), is internally polled at the start of every multiframe (this occurs every 5 ms and the device can be programmed to give an interrupt at the start of every multiframe), and its contents are interpreted as subchannel 1. If multiframing is enabled and the contents of BR2(7:4) have not been updated, then the subchannel is re–transmitted as is. BR2(7:4) can be updated any time between the 5 ms interrupts. BR2(7:4) are read/write bits. Application of either a software or hardware reset resets these bits to all 0s. Note that BR2(7) is the MSB of SC1 and BR2(4) is the LSB. Refer to Section 10 for a more detailed description of this feature.

**TE: Q Nibble to S/T Loop** — BR2(7:4) are used for multiframing. In the TE mode of operation these four bits correspond to the Q channel data for transmission to the NT. When multiframing is enabled, the TE will transmit the bits in BR2(7:4), as Q channel data, in accordance with CCITT I.430, ETSI ETS 300012, and ANSI T1.605. BR2(7:4) is internally polled at the start of every multiframe (this occurs every 5 ms and the device can be programmed to give an interrupt at the start of every multiframe), and its contents are interpreted as Q channel data. If multiframing is enabled and the contents of BR2(7:4) have not been updated then the Q channel is re–transmitted as is. BR2(7:4) can be updated any time between the 5 ms interrupts. BR2(7:4) are read/write bits. Application of either a software or hardware reset sets these bits to all 1s. Note that BR2(7) is the MSB of the Q channel and BR2(4) is the LSB. Refer to Section 10 for a more detailed description of this feature.

## 9.5 BR3

| | (7) | (6) | (5) | (4) | (3) | (2) | (1) | (0) |
|---|---|---|---|---|---|---|---|---|
| **BR3** | NT: Q.1<br>TE: SC1.1 | NT: Q.2<br>TE: SC1.2 | NT: Q.3<br>TE: SC1.3 | NT: Q.4<br>TE: SC1.4 | NT: Q Qual<br>TE: Not Applicable | Interrupt Every Multiframe | | |

**BR3(7:4)**

**NT: Q Nibble from S/T Loop** — BR3(7:4) are used in the multiframing mode of operation. When the device is configured as an NT and multiframing has been enabled, these bits correspond to the received Q channel nibble from the TE(s). These bits are updated once every multiframe. The NT–configured device can give an interrupt once every multiframe (see BR3(2) and NR4(2)) or every time a new Q channel nibble is received. BR3(7:4) are read only bits. Application of either a hardware

or software reset sets these bits to all 1s. Note that BR3(7) is the MSB of the received Q channel nibble, and BR3(4) is the LSB. Refer to Section 12 for a more detailed description of this feature. Reading BR3 clears the multiframe interrupt.

**TE: SC1 FROM S/T LOOP** — BR3(7:4) are used in the multiframing mode of operation. When the device is configured as a TE and multiframing has been enabled, these bits correspond to the received subchannel 1 nibble from the NT. These bits are updated once every multiframe. The TE–configured device can give an interrupt once every multiframe, or every time a new subchannel nibble (SC1) is received (see BR3(2) and NR4(2)). BR3(7:4) are read only bits. Application of either a hardware or software reset resets these bits to all 0s. Note that BR3(7) is the MSB of the received SC1 subchannel nibble and BR3(4) is the LSB. Refer to Section 12 for a more detailed description of this feature.

**BR3(3) — NT: Q Bit Quality Indicate**
**TE: Not Applicable**

In the NT mode, this bit corresponds to the Q bit quality indication. When multiframing has been initiated by the NT, the TE(s) will respond by sending Q data once every five frames. This Q data will be transmitted in the Fa bit position. During the other four frames (i.e., when the TE(s) are not transmitting Q data), the Fa bit should be a 0. BR3(3) being high indicates that the Fa bits in the frames where multiframing data was not being transmitted were 0s. This bit is a read only bit and is reset to 0 by application of either a hardware or software reset.

**BR3(2)**

**NT: Interrupt Every Multiframe** — Programming of BR3(2) dictates whether an interrupt will be given every multiframe (assuming multiframing has been enabled and IRQ2 enable, NR4(2), has been set), or only on the receipt of a new Q channel nibble from the TE(s). When BR3(2) is 1, an interrupt is given every multiframe. When BR3(2) is 0, an interrupt is given only on the receipt of a new Q channel nibble. Refer to Section 12 for a more detailed description. BR3(2) is a read/write bit and is reset to 0 by application of either a hardware or software reset.

**TE: Interrupt Every Multiframe** — Programming of BR3(2) dictates whether an interrupt will be given every multiframe (assuming multiframing has been enabled and IRQ2 enable, NR4(2), has been set), or only on the receipt of a new SC1 subchannel nibble from the NT. When BR3(2) is 1, an interrupt is given every multiframe. When BR3(2) is 0, an interrupt is given only on the receipt of a new SC1 subchannel nibble. Refer to Section 12 for a more detailed description. BR3(2) is a read/write bit and is reset to 0 by application of either a hardware or software reset.

## 9.6 BR4

| | (7) | (6) | (5) | (4) | (3) | (2) | (1) | (0) |
|---|---|---|---|---|---|---|---|---|
| **BR4** | FV7 | FV6 | FV5 | FV4 | FV3 | FV2 | FV1 | FV0 |

Recommendation CCITT I.430, ETSI ETS 300012, and ANSI T1.605 specifications state that there must be two AMI violations in every S/T frame. The F bit is the first violation and the succeeding violation must occur within 13 or 14 bauds, depending on the configuration of the transceiver as either an NT or TE. BR4(7:0) is the output of an 8–bit binary counter. This counter counts the number of frames which do not contain the correct number of AMI violations. Note that in multiframing, it is possible to have a frame which does not contain the correct number of violations (Fa = 1, B1 = 1). The MC145574, when in multiframe mode, does not count these frames. Thus, this counter is a “frame error” counter, counting the number of frames which do not contain the correct number of AMI violations. BR4(7:0) only counts frames not containing the correct number of AMI violations after FSYNC has been achieved, and ceases counting whenever FSYNC is lost.

BR4(7:0) is applicable to both NT and TE modes of operation. It is a read/write register, thereby allowing the user to program the counter to a predetermined value. The counter is initialized to “100” by a hardware/software reset. Note that the counter, upon reaching a value of “FF”, will not roll over; i.e., it will remain at “FF” until the user rewrites a starting value. Note that BR4(7) is the MSB of the counter and BR4(0) is the LSB.

## 9.7 BR5

| | (7) | (6) | (5) | (4) | (3) | (2) | (1) | (0) |
|---|---|---|---|---|---|---|---|---|
| **BR5** | BPV7 | BPV6 | BPV5 | BPV4 | BPV3 | BPV2 | BPV1 | BPV0 |

BR5(7:0) is the output of an 8–bit binary counter. This counter counts the number of unbalanced frames. A frame in which the total number of positive pulses is different from the total number of negative pulses constitutes an unbalanced frame. BR5(7:0) is applicable to both NT and TE modes of operation. It is a read/write register, thereby allowing the user to program the counter to a predetermined value. The counter is initialized to “100” by a hardware/software reset. Note that the counter, upon reaching a value of “FF”, will not roll over; i.e., it will remain at “FF” until the user rewrites a starting value. Note that BR5(7) is the MSB of the counter and BR5(0) is the LSB.

## 9.8 BR6

| | (7) | (6) | (5) | (4) | (3) | (2) | (1) | (0) |
|---|---|---|---|---|---|---|---|---|
| **BR6** | B1 S/T Loopback Transparent | B1 S/T Loopback Non–Transparent | B2 S/T Loopback Transparent | B2 S/T Loopback Non–Transparent | IDL2 B1 Loopback Transparent | IDL2 B1 Loopback Non–Transparent | IDL2 B2 Loopback Transparent | IDL2 B2 Loopback Non–Transparent |

**BR6(7) — B1 S/T Loopback Transparent**

This bit is a read/write bit and is applicable to both NT and TE modes of operation. When this bit is 0, the device functions normally. When this bit is 1, the device enters a “B1 S/T Loopback Transparent Mode”. In this mode, data entering the device from RxP/PxN in the B1 timeslot is demodulated and remodulated back out on TxP/TxN in the B1 timeslot. The demodulated B1 data continues to present itself on IDL2 Tx in the B1 timeslot (hence, the term “transparent”). Data entering the part from IDL2 Rx in the B1 timeslot is ignored. This bit is reset to 0 by either a software reset, a hardware reset, or in the “return to normal” mode (NR0(0) = 1).

**BR6(6) — B1 S/T Loopback Non–Transparent**

This bit is a read/write bit and is applicable to both NT and TE modes of operation. When this bit is 0 the device functions normally. When this bit is 1, the device enters a “B1 S/T Loopback Non–Transparent Mode”. In this mode, data entering the device from RxP/RxN in the B1 timeslot is demodulated and remodulated back out on TxP/TxN in the B1 timeslot. Data entering the part from IDL2 Rx in the B1 timeslot is ignored. IDL2 Tx ignores the demodulated B1 data, presenting in its stead the “idle 1s” condition in the IDL2 Rx B1 timeslot (hence, the term “non–transparent”). This bit is reset to 0 by either a software reset, a hardware reset, or in the “return to normal” mode (NR0(0) = 1).

**BR6(5) — B2 S/T Loopback Transparent**

This bit is a read/write bit and is applicable to both NT and TE modes of operation. When this bit is 0, the device functions normally. When this bit is 1, the device enters a “B2 S/T Loopback Transparent Mode”. In this mode, data entering the device from RxP/RxN in the B2 timeslot is demodulated and remodulated back out on TxP/TxN in the B2 timeslot. The demodulated B2 data continues to present itself on IDL2 Tx in the B2 timeslot (hence, the term “transparent”). Data entering the part from IDL2 Rx in the B2 timeslot is ignored. This bit is reset to 0 by either a software reset, a hardware reset, or in the “return to normal” mode (NR0(0) = 1).

**BR6(4) — B2 S/T Loopback Non–Transparent**

This bit is a read/write bit and is applicable to both NT and TE modes of operation. When this bit is 0, the device functions normally. When this bit is 1, the device enters a “B2 S/T Loopback Non–Transparent Mode”. In this mode, data entering the device from RxP/RxN in the B2 timeslot is demodulated and remodulated back out of TxP/TxN in the B2 timeslot. Data entering the part from IDL2 Rx in the

B2 timeslot is ignored. IDL2 Tx ignores the demodulated B2 data, presenting in its stead the “idle 1s” condition in the IDL2 Rx B2 timeslot (hence, the term “non–transparent”). This bit is reset to 0 by either a software reset, a hardware reset, or in the “return to normal” mode (NR0(0) = 1).

**BR6(3) — IDL2 B1 Loopback Transparent**

This bit is a read/write bit and is applicable to both NT and TE modes of operation when the MC145574 is configured for GCI or IDL2 type interfaces. When this bit is a 0, the MC145574 operates normally. When this bit is a 1, the MC145574 internally loops back the data received during the B1 timeslot at $D_{in}$ and transmits it onto the $D_{out}$ pin during the B1 timeslot. Data entering the $D_{in}$ pin during the B1 timeslot is also transmitted onto the S/T–interface. This bit is reset to 0 by either a software reset, a hardware reset, or in the “return to normal” mode (NR0(0) = 1).

**BR6(2) — IDL2 B1 Loopback Non–Transparent**

This bit is a read/write bit and is applicable to both NT and TE modes of operation when the MC145574 is configured for GCI or IDL2 type interfaces. When this bit is a 0, the MC145574 operates normally. When this bit is a 1, the MC145574 internally loops back the data received during the B1 channel timeslot at $D_{in}$ and transmits it onto the $D_{out}$ pin during the B1 timeslot. Data entering the $D_{in}$ pin during the B1 timeslot is not transmitted onto the S/T–interface. Instead, the MC145574 transmits idle 1s onto the B1 channel bits of the S/T–interface. This bit is reset to 0 by either a software reset, a hardware reset, or in the “return to normal” mode (NR0(0) = 1).

**BR6(1) — IDL2 B2 Loopback Transparent**

This bit is a read/write bit and is applicable to both NT and TE modes of operation when the MC145574 is configured for GCI or IDL2 type interfaces. When this bit is a 0, the MC145574 operates normally. When this bit is a 1, the MC145574 internally loops back the data received during the B2 channel timeslot at $D_{in}$ and transmits it onto the $D_{out}$ pin during the B2 timeslot. Data entering the $D_{in}$ pin during the B2 timeslot is also transmitted onto the S/T–interface. This bit is reset to 0 by either a software reset, a hardware reset, or in the “return to normal” mode (NR0(0) = 1).

**BR6(0) — IDL2 B2 Loopback Non–Transparent**

This bit is a read/write bit and is applicable to both NT and TE modes of operation when the MC145574 is configured for GCI or IDL2 type interfaces. When this bit is a 0, the MC145574 operates normally. When this bit is a 1, the MC145574 internally loops back the data received during the B2 channel timeslot at $D_{in}$ and transmits it onto the $D_{out}$ pin during the B2 timeslot. Data entering the $D_{in}$ pin during the B2 timeslot is not transmitted onto the S/T–interface. Instead, the MC145574 transmits idle 1s onto the B2 channel bits of the S/T–interface. This bit is reset to 0 by either a software reset, a hardware reset, or in the “return to normal” mode (NR0(0) = 1).

## 9.9 BR7

| | (7) | (6) | (5) | (4) | (3) | (2) | (1) | (0) |
|---|---|---|---|---|---|---|---|---|
| **BR7** | Activation Procedures Disabled | NT: Active Only NT Enable TE: D Channel Procedures Ignored | NT: Enable Multi–framing TE: Not Applicable | NT: Invert E Channel TE: Map E To IDL2 | NT: IDL2 Master Mode TE: IDL2 Free Run | IDL2 Clock Speed (LSB) | LAPD Polarity Control | NT: Activation Timer #2 Expired TE: Not Applicable |

**BR7(7) — Activation Procedures Disabled**

This bit a read/write bit and is applicable to both NT and TE modes of operation. When this bit is 0, the MC145574 functions normally. When this bit is set to 1, the transmit section of the transceiver is forced into the highest information state. Thus, if the device is operating as NT, INFO 4 is forced out on the transmit side of the device. INFO 4 is forced out regardless of what is being received on RxP/RxN. If the device is operating as a TE, the transceiver transmits INFO 3 on TxP/TxN.

Note that if activation procedures are disabled as a TE, causing INFO 3 to be transmitted, then this state may or may not be commensurate with receiving INFO 0 from the NT. In the event that INFO 0 is being received, the transmitted INFO 3 is transmitted asynchronously. If either INFO 2 or INFO 4 are subsequently received, then the TE's INFO 3 aligns itself to the received signal in accordance with CCITT I.430, ETSI ETS 300012, and ANSI T1.605. Note also that a TE wakes up if it receives either INFO 2 or INFO 4 from the NT. However, an NT transmitting INFO 0 will not wake up to the reception of INFO 3 from the TE. For an NT to be woken up by a TE, it must first receive INFO 1 from the TE and then proceed to go through the subsequent handshaking. BR7(7) is reset to 0 by application of either a hardware or software reset.

**BR7(6) — NT: Active Only NT Enable**
**TE: D Channel Procedures Ignored**

When the MC145574 is configured as a TE, this bit is used to enable/disable D channel contention procedures in accordance with the CCITT I.430, ETSI ETS 300012, and ANSI T1.605. When this bit is 0, the D channel procedures are adhered to as per the DREQUEST, DGRANT, and CLASS pin descriptions. When this bit is 1, the D channel procedures are ignored, allowing the data present in the D channel on IDL2 Rx to be modulated regardless of the status of DREQUEST and DGRANT. BR7(6) = 1 causes the TE to disregard the demodulated E echo bits. The TE's D data will be modulated regardless. This bit is a read/write bit and is reset to 0 by application of either a software or a hardware reset. When configured as an NT, this bit enables the "active only NT" mode. In this mode, the NT is restricted to the G2 or G3 state; i.e., the device is either activated or attempting to activate. The device is never allowed to fully deactivate.

**BR7(5) — NT: Enable Multiframing**
**TE: Not Applicable**

When the MC145574 is configured as an NT, this bit is used to enable/disable multiframing in accordance with CCITT I.430, ETSI ETS 300012, and ANSI T1.605. When this bit is 0, multiframing is disabled. In this mode the M, Fa, and S bauds transmitted from the NT will be binary 0. When this bit is 1, multiframing is enabled. In this mode, the M, Fa, and S bauds will adhere to the multiframing coding rules as outlined in CCITT I.430 and ANSI T1.605. Since the TE cannot initiate multiframing, this bit has no application in this mode. This bit is a read/write bit and is reset to 0 by application of either a software or a hardware reset.

**BR7(4)**

**NT: Invert Echo Channel** — When the MC145574 is configured as an NT, this bit is used to determine the polarity of the transmitted echo channel from the NT to the TE. When this bit is a 0, the transmitted E bit is the same as the previously demodulated D bit from the TE(s). When this bit is 1, the transmitted E bit is the logical inverse of the previously demodulated D bit. This bit is a read/write bit and is reset to 0 by application of either a software or hardware reset.

**TE: Map E Bits to IDL2** — With the MC145574 configured as a TE and this bit a 0, the TE outputs the demodulated D channel data in the D timeslot on the IDL2 Tx. When this bit is set to 1, the TE outputs the demodulated E channel in the D timeslot on IDL2 Tx, neglecting the demodulated D channel data. This bit is a read/write bit and is reset to 0 by application of either a software or a hardware reset.

**BR7(3)**

**NT: IDL2 Master Mode** — With the MC145574 configured as an NT, this bit determines whether the device operates in IDL2 slave or IDL2 master mode. When this bit is 0, the NT operates in the IDL2 slave mode, where IDL2 SYNC and IDL2 CLK are inputs to the device. When this bit is 1, the NT operates in the NT IDL2 master mode, where IDL2 SYNC and IDL2 CLK are outputs from the device. This bit is a read/write bit OR'd with the M/$\overline{S}$ pin and is reset to 0 by application of either a software or hardware reset.

**TE: IDL2 Free Run** — When the MC145574 is configured as a TE and the loop is active, the device will output IDL2 SYNC and IDL2 CLK synchronous to the inbound data from the NT. When the loop is inactive and this bit is 0, the TE does not output IDL2 SYNC or IDL2 CLK. If this bit is 1, the TE outputs IDL2 SYNC and IDL2 CLK regardless of the status of the loop. If the loop is inactive, these

signals will be free–running (derived from the crystal). If the loop is active, these signals will be synchronous to the inbound data. This bit is a read/write bit and is reset to 0 by application of either a software or a hardware reset.

**BR7(2) — IDL2 Clock Speed (LSB)**

This bit is a read/write bit and is applicable to both NT and TE modes of operation. BR7(2), in conjunction with BR13(5), determines the IDL2 CLK frequency when operating in the IDL2 master mode. BR7(2) is the LSB and BR13(5) is the MSB. The code corresponding to each IDL2 clock frequency is shown in Table 9–4.

**Table 9–4. IDL2 Clock Speed Codes**

| BR13(5) | BR7(2) | IDL2 CLK | |
|---|---|---|---|
| | | Rate | Duty Cycle |
| 0 | 0 | 2.56 MHz | 50% |
| 0 | 1 | 2.048 MHz | 53.3% |
| 1 | 0 | 1.536 MHz | 50% |
| 1 | 1 | 512 kHz | 50% |

Application of either a hardware or a software reset will reset this bit to 0. Refer to Section 4 for a more detailed description of this feature.

**BR7(1) — NT: LAPD Polarity Control (NT Terminal Mode)**
**TE: LAPD Polarity Control**

When the MC145574 is configured as a TE or an NT (Terminal Mode), this bit performs the “LAPD Polarity Control” function. When this bit is 0, the active state of DREQUEST and DGRANT signals is defined to be the logic 1 or high state. When this bit is 1, the active state of these signals is defined to be the logic 0 or low state. This bit is a read/write bit and is reset to 0 by application of either a hardware or software reset.

**BR7(0) — NT: Activation Timer #2 Expired**
**TE: Not Applicable**

When the MC145574 is configured as an NT, this bit performs the “Activation Timer #2 Expired” function. When this bit is 0, the NT–configured S/T transceiver uses a value of 50 ms for the Timer #2 value outlined in CCITT I.430, ETSI ETS 300012, and ANSI T1.605 (i.e., the device unambiguously detects INFO 1). When this bit is 1, a value of 100 ms is used for the value of Timer #2. This bit is a read/write bit and is reset to 0 by application of either a hardware or software reset.

## 9.10 BR8

The functions that were related to the IDL2 A/M FIFOs have been removed. Writing to these registers will have no effect, and reading them will return 00H or any value that has been written to them. (No register shown.)

## 9.11 BR9

| | (7) | (6) | (5) | (4) | (3) | (2) | (1) | (0) |
|---|---|---|---|---|---|---|---|---|
| **BR9** | NT: TXSC2.1 TE: RXSC2.1 | NT: TXSC2.2 TE: RXSC2.2 | NT: TXSC2.3 TE: RXSC2.3 | NT: TXSC2.4 TE: RXSC2.4 | NT: TXSC3.1 TE: RXSC3.1 | NT: TXSC3.2 TE: RXSC3.2 | NT: TXSC3.3 TE: RXSC3.3 | NT: TXSC3.4 TE: RXSC3.4 |

**BR9(7:4)**

**NT: SC2 to Loop** — BR9(7:4) is used for multiframing. In the NT mode of operation, these four bits correspond to subchannel 2 for transmission to the TE(s). Multiframing is initiated by the NT by setting BR7(5). When multiframing is enabled, the NT will transmit the bits in BR9(7:4) as subchannel 2, in accordance with CCITT I.430, ETSI ETS 300012, and ANSI T1.605. BR9(7:4), are internally polled at the start of every multiframe (this occurs every 5 ms and the device can be programmed to give an interrupt at the start of every multiframe), and the contents are interpreted as subchannel 2. If multiframing is enabled and the contents of BR9(7:4) have not been updated, the subchannel is re–transmitted as is. BR9(7:4) can be updated any time between the 5 ms interrupts. In the NT mode of operation, BR9(7:4) are write only bits. These bits are reset to 0 by application of either a software or hardware reset. Note that BR9(7) is the MSB of SC2 and BR9(4) is the LSB. Refer to Section 10 for a detailed description of the multiframe procedure.

**TE: SC2 from Loop** — BR9(7:4) are used in the multiframing mode of operation. When the device is configured as a TE and multiframing has been enabled, these bits correspond to the received subchannel 2 nibble from the NT. These bits are updated once every multiframe. BR9(7:4) are read only bits and are reset to 0 by application of either a software or hardware reset. Note that BR9(7) is the MSB of SC2 and BR9(4) is the LSB. Refer to Section 10 for a detailed description of the multiframe procedure.

**BR9(3:0)**

**NT: SC3 to Loop** — BR9(3:0) is used for multiframing. In the NT mode of operation, these four bits correspond to subchannel 3 for transmission to the TE(s). When multiframing is enabled, the NT will transmit the bits in BR9(3:0) as subchannel 3, in accordance with CCITT I.430, ETSI ETS 300012, and ANSI T1.605. BR9(3:0) are internally polled at the start of every multiframe (this occurs every 5 ms and the device can be programmed to give an interrupt at the start of every multiframe), and the contents are interpreted as subchannel 3. If multiframing is enabled and the contents of BR9(3:0) have not been updated, the subchannel is re–transmitted as is. BR9(3:0) can be updated any time between the 5 ms interrupts. In the NT mode of operation, BR9(3:0) are write only bits. These bits are reset to 0 by application of either a software or hardware reset. Note that BR9(3) is the MSB of SC3 and BR9(0) is the LSB. Refer to Section 12 for a detailed description of the multiframe procedure.

**TE : SC3 from Loop** — BR9(3:0) are used in the multiframing mode of operation. When the device is configured as a TE and multiframing has been enabled, these bits correspond to the received subchannel 3 nibble from the NT. These bits are updated once every multiframe. BR9(3:0) are read only bits and are reset to 0 by application of either a software or hardware reset. Note that BR9(3) is the MSB of SC2 and BR9(0) is the LSB. Refer to Section 10 for a detailed description of the multiframe procedure.

## 9.12 BR10

| | (7) | (6) | (5) | (4) | (3) | (2) | (1) | (0) |
|---|---|---|---|---|---|---|---|---|
| **BR10** | NT: TXSC4.1 TE: RXSC4.1 | NT: TXSC4.2 TE: RXSC4.2 | NT: TXSC4.3 TE: RXSC4.3 | NT: TXSC4.4 TE: RXSC4.4 | NT: TXSC5.1 TE: RXSC5.1 | NT: TXSC5.2 TE: RXSC5.2 | NT: TXSC5.3 TE: RXSC5.3 | NT: TXSC5.4 TE: RXSC5.4 |

**BR10(7:4)**

**NT: SC4 to Loop** — BR10(7:4) are used for multiframing. In the NT mode of operation, these four bits correspond to subchannel 4 for transmission to the TE(s). When multiframing is enabled, the NT will transmit the bits in BR10(7:4) as subchannel 4, in accordance with CCITT I.430, ETSI ETS 300012, and ANSI T1.605. BR10(7:4) are internally polled at the start of every multiframe (this occurs every 5 ms and the device can be programmed to give an interrupt at the start of every multiframe), and the contents are interpreted as subchannel 4. If multiframing is enabled and the contents of BR10(7:4) have not been updated, the subchannel is re–transmitted as is. BR10(7:4) can be updated any time between the 5 ms interrupts. In the NT mode of operation, BR10(7:4) are write only bits. These bits

are reset to 0 by application of either a software or hardware reset. Note that BR10(7) is the MSB of SC4 and BR10(4) is the LSB. Refer to Section 10 multiframing for a detailed description of the multiframing procedure.

**TE: SC4 from Loop** — BR10(7:4) are used in the multiframing mode of operation. When the device is configured as a TE and multiframing has been enabled, these bits correspond to the received subchannel 4 nibble from the NT. These bits are updated once every multiframe. BR10(7:4) are read only bits and are reset to 0 by either a software or hardware reset. Note that BR10(7) is the MSB of SC4 and BR10(4) is the LSB. Refer to Section 10 for a detailed description of multiframe procedures.

**BR10(3:0)**

**NT: SC5 to Loop** — BR10(3:0) are used for multiframing. In the NT mode of operation, these four bits correspond to subchannel 5 for transmission to the TE(s). When multiframing is enabled, the NT will transmit the bits in BR10(3:0) as subchannel 5, in accordance with CCITT I.430, ETSI ETS 300012, and ANSI T1.605. BR10(3:0) is internally polled at the start of every multiframe (this occurs every 5 ms and the device can be programmed via NR4(2) to give an interrupt at the start of every multiframe), and the contents are interpreted as subchannel 5. If multiframing is enabled and the contents of BR10(3:0) have not been updated, the subchannel is re–transmitted as is. BR10(3:0) can be updated any time between the 5 ms interrupts. In the NT mode of operation, BR10(3:0) are write only bits. These bits are reset to 0 by application of either a software or hardware reset. Note that BR10(3) is the MSB of SC5 and BR10(0) is the LSB. Refer to Section 10 for a detailed description of the multiframe procedure.

**TE: SC5 from Loop** — BR10(3:0) are used in the multiframing mode of operation. When the device is configured as a TE and multiframing has been enabled, these bits correspond to the received subchannel 5 nibble from the NT. These bits are updated once very multiframe. BR10(3:0) are read only bits and are reset to 0 by either a software or hardware reset. Note that BR10(3) is the MSB of SC5 and BR10(0) is the LSB. Refer to Section 10 for a detailed description of the multiframe procedure.

## 9.13 BR11

| | (7) | (6) | (5) | (4) | (3) | (2) | (1) | (0) |
|---|---|---|---|---|---|---|---|---|
| **BR11** | NT: Do Not React To INFO 1 TE: Not Applicable | NT: Do Not React To INFO 3 TE: Not Applicable | Rx INFO State B1 | Rx INFO State B0 | Tx INFO State B1 | Tx INFO State B0 | External S/T Loopback | Transmit 96 kHz Test Signal |

### 9.13.1 BR11(7) — NT: Do Not React to INFO 1 TE: Not Applicable

This bit is only applicable to the NT mode of operation. When this bit is 0, the part functions normally. When this bit is 1, the NT will not react to INFO 1 from the TE. (Note, however, that the NT will give an interrupt indicating a change in received information state.) Only when the NT resets this bit to 0 will it react to INFO 1. This feature is used in the NT in applications where it is necessary to delay activation of the S/T loop until the U link has reached its active state. This bit is a read/write bit and is reset to 0 by application of either a hardware or software reset.

### BR11(6) — NT: Do Not React to INFO 3 TE: Not Applicable

This bit is only applicable to the NT mode of operation. When this bit is 0, the part functions normally. When this bit is 1, the NT will not react to INFO 3 from the TE (this INFO 3 from the TE being the response of the TE to INFO 2 from the NT). Only when the NT resets this bit to 0 will it react to INFO 3. In the meantime, the NT will continue to transmit INFO 2. This feature is used in the NT in applications where it is necessary to delay activation of the S/T loop until the U link has reached its active state. This bit is a read/write bit and is reset to 0 by application of either a hardware or software reset.

**BR11(5), BR11(4) — Rx INFO State B1 and B0**

These bits are read/write bits and are applicable to both NT and TE modes of operation. The MC145574 internally sets these bits to indicate the status of the received signal; i.e., it is INFO 0, 1, 2, 3, 4, or X, where INFO X is none of the above. An example of INFO X would be when it is receiving the 96 kHz test signal. Another example of INFO X would be where the transceiver is not receiving INFO 0, but it has not yet determined whether it is INFO 1, 2, 3, or 4.

The codes corresponding to the different states are shown in Table 9–5.

**Table 9–5. BR11(5), BR11(4) Rx INFO State Codes**

| BR11(5) | BR11(4) | Receive Information State |
|---|---|---|
| 0 | 0 | INFO 0 |
| 0 | 1 | INFO LOW |
| 1 | 0 | INFO HIGH |
| 1 | 1 | INFO X |

NOTE: When configured as an NT, receiving INFO LOW corresponds to receiving INFO 1, and receiving INFO HIGH corresponds to receiving INFO 3. Conversely, when the device is operating as a TE, receiving INFO LOW corresponds to receiving INFO 2, and receiving INFO HIGH corresponds to receiving INFO 4. The device internally sets these bits, and this internal write overrides any external write. These bits are reset to 0 by application of either a hardware or software reset.

**BR11(3), BR11(2) — Tx INFO State B1 and B0**

These bits are read/write bits and are applicable to both NT and TE modes of operation. The MC145574 internally sets these bits to indicate the status of the transmitted signal; i.e., is it INFO 0, 1, 2, 3, 4, or X where INFO X is none of the above. An example of INFO X would be when it is transmitting the 96 kHz test signal. The codes corresponding to the different states is shown in Table 9–6.

**Table 9–6. BR11(3), BR11(2) Tx INFO State Codes**

| BR11(3) | BR11(2) | Transmit Information State |
|---|---|---|
| 0 | 0 | INFO 0 |
| 0 | 1 | INFO LOW |
| 1 | 0 | INFO HIGH |
| 1 | 1 | INFO X |

NOTE: When configured as an NT, transmitting INFO LOW corresponds to transmitting INFO 2, and transmitting INFO HIGH corresponds to transmitting INFO 4. Conversely, when the device is operating as a TE, transmitting INFO LOW corresponds to transmitting INFO 1, and transmitting INFO HIGH corresponds to transmitting INFO 3. The device internally sets these bits, and this internal write overrides any external write. These bits are reset to 0 by application of either a hardware or software reset.

**BR11(1) — External S/T Loopback**

This bit is a read/write bit and is applicable to both NT and TE modes of operation. When this bit is 0, the MC145574 functions normally. If the transmit pair is shorted to the receive pair while this bit is 1, the device will perform an external or “analog” loopback. In an analog loopback, the device demodulates its own transmitted data. The transceiver should have its activation procedures disabled (BR7(7) = 1) and be configured for the IDL2 master mode (BR7(3) = 1). This feature is useful for test purposes. In external loopback, the B1 and B2 channels are looped back. In the NT mode, the D channel is also looped back. The D channel is not looped back in the TE mode. Application of a hardware or software reset will reset this bit to 0.

**BR11(0) — Transmit 96 kHz Test Signal**

This bit is a read/write bit and is applicable to both NT and TE modes of operation. When this bit is 0, the MC145574 functions normally. When this bit is 1, the device transmits a 96 kHz square wave test signal on TxP/TxN. This test signal can be used for test purposes. This 96 kHz test signal qualifies as a “Transmit INFO X” state. Correspondingly, the MC145574 receiving the 96 kHz test signal will be in the “Receive INFO X” state. Application of a hardware or software reset will reset this bit to 0.

## 9.14 BR12

| | (7) | (6) | (5) | (4) | (3) | (2) | (1) | (0) |
|---|---|---|---|---|---|---|---|---|
| **BR12** | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved |

Byte register 12 is reserved for Motorola use only.

## 9.15 BR13

| | (7) | (6) | (5) | (4) | (3) | (2) | (1) | (0) |
|---|---|---|---|---|---|---|---|---|
| BR13 | NT: NT1 Star Mode TE: Not Applicable | Reserved | IDL2 Clock Speed (MSB) | Mute B2 on IDL2 Tx | Mute B1 on IDL2 Tx | NT: Force Echo Channel to Zero TE: Not Applicable | NT: Not Applicable TE: Force IDL2 Tx | Reserved |

**BR13(7) — NT: NT1 Star Mode**
**TE: Not Applicable**

This bit is a read/write bit and is only applicable to the NT mode of operation. When this bit is 0, the device functions normally. When this bit is 1, the device is configured for NT1 Star mode operation. Refer to Section 11 for a detailed description of this mode. This bit is reset to 0 by application of either a hardware or software reset.

**BR13(6)**

This bit has no function and is reserved for Motorola use only.

**BR13(5) — IDL2 Clock Speed (MSB)**

This bit is a read/write bit and is applicable to both NT and TE modes of operation. BR13(5), in conjunction with BR7(2), determines the IDL2 CLK frequency when operating in the IDL2 master mode. BR7(2) is the LSB and BR13(5) is the MSB. The code corresponding to each IDL2 clock frequency is as shown in the description for BR7(2). Application of either a hardware or a software reset will reset this bit to 0. See Table 9–3.

**BR13(4) — Mute B2 on IDL2**

This bit is a read/write bit and is applicable to both NT and TE modes of operation. When this bit is 0, the device functions normally. When this bit is 1, the data transmitted on the B2 channel on IDL2 Tx will be forced to the “idle 1s” condition. This feature is primarily used in the NT1 Star mode operation. Refer to Section 11 for a detailed description of this mode. Application of a hardware or software reset resets this bit to 0.

**BR13(3) — Mute B1 on IDL2**

This bit is a read/write bit and is applicable to both NT and TE modes of operation. When this bit is 0, the device functions normally. When this bit is 1, the data transmitted on the B1 channel on IDL2 Tx will be forced to the “idle 1s” condition. This feature is primarily used in the NT1 Star mode operation.

Refer to Section 11 for a detailed description of this mode. Application of a hardware or software reset resets this bit to 0.

**BR13(2) — NT: Force Echo Channel to Zero**
**TE: Not Applicable**

This bit is a read/write bit and is only applicable to the NT mode of operation. When the MC145574 is configured as an NT and this bit is 0, the device functions normally. When this bit is 1, the NT forces the transmitted E bits to be 0. This feature is used for test purposes when the NT wishes to communicate to the TEs on the passive bus that they should disengage from the D channel. Application of either a hardware or a software reset resets this bit to 0.

**BR13(1) —NT: Not Applicable**
**TE: Force IDL2 Tx**

This bit is a read/write bit and is only applicable to the TE mode of operation. When the MC145574 is configured as a TE and this bit is 0, the device functions normally. When this bit is 1, data is presented on IDL2 Tx in the special case where the TE is synchronized to INFO 4 incoming from the NT but its transmitter is not fully active (i.e., not transmitting INFO 3). This feature is useful when the MC145574 is in the transmit power down mode (NR0(2) = 1) and it is desired to continue to process data from the NT. This bit has no effect when the device is fully active (transmitting INFO 3 and receiving INFO 4). When BR13(1) = 0 and the device is not fully active, “idle 1s” will be presented on IDL2 Tx. Application of either a hardware or a software reset resets this bit to 0.

**BR13(0)**

This bit is reserved.

## 9.16 BR14

| | (7) | (6) | (5) | (4) | (3) | (2) | (1) | (0) |
|---|---|---|---|---|---|---|---|---|
| **BR14** | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved |

Byte register 14 is a read/write register. It is reserved for Motorola use only.

## 9.17 BR15

| | (7) | (6) | (5) | (4) | (3) | (2) | (1) | (0) |
|---|---|---|---|---|---|---|---|---|
| **BR15** | Overlay Register Enabled | | Rev 5 | Rev 4 | Rev 3 | Rev 2 | Rev 1 | Rev 0 |

**BR15(7) — Overlay Register Enabled**

When the device is initialized, this bit is a logic 0. When set to a logic 0, operation of the MC145574 register map is identical to that of the MC145474. When set to a logic 1, a second set overlay register is enabled. The overlay register map allows access to the TSA registers required by the IDL2 and also to a GCI control register.

**BR15(5:0) — Device Revision Identification, Rev (5:0)**

The Rev (5:0) bits indicate the revision status of the device. These bits are read only and can only be modified by altering the device mask. Rev (5:0) is set to 11H for G20R1 mask set and to 03H for F57J4 mask set. See Section 20 for F57J4 mask set differences.

# 10
# OVERLAY REGISTER MAP DEFINITION

## 10.1 INTRODUCTION

There are eleven overlay registers (OR0 through OR9 and OR15) in the MC145574. The overlay registers are a second bank of registers available when the overlay register control bit BR15(7) is set to a logic 1. These overlay registers are in the IDL2 TSA mode used to assign the timeslot used by each channel (B1, B2, and D) for transmission and reception; OR0 through OR5, OR6, OR7, and OR8 are control registers used in the GCI indirect mode, and OR15 gives the revision number of the S/T chip.

**Table 10–1. Overlay Register Map**

| | (7) | (6) | (5) | (4) | (3) | (2) | (1) | (0) |
|---|---|---|---|---|---|---|---|---|
| **OR0** | $D_{in}$ B1 Channel Timeslot Bits (7:0) (IDL2 Mode) | | | | | | | |
| **OR1** | $D_{in}$ B2 Channel Timeslot Bits (7:0) (IDL2 Mode) | | | | | | | |
| **OR2** | $D_{in}$ D Channel Timeslot Bits (7:0) (IDL2 Mode) | | | | | | | |
| **OR3** | $D_{out}$ B1 Channel Timeslot Bits (7:0) (IDL2 Mode) | | | | | | | |
| **OR4** | $D_{out}$ B2 Channel Timeslot Bits (7:0) (IDL2 Mode) | | | | | | | |
| **OR5** | $D_{out}$ D Channel Timeslot Bits (7:0) (IDL2 Mode) | | | | | | | |
| **OR5** | Time Slot Assignment for GCI Mode | | | | | S2 | S1 | S0 |
| **OR6** | TSA B1 Enable | TSA B2 Enable | TSA D Enable | | $D_{out}$ Open Drain | GCI Indirect Mode Enable | CLK1 | CLK0 |
| **OR7** | Disable 3 V Regulator | Enable S/G Bit | Enable TCLK | Dual Frame Syncs | Long Frame | 8/10 Bit Select | $\overline{\text{TSEN}}$ B1/B2 Enable, BCL Enable | $\overline{\text{TSEN}}$ D Channel Enable |
| **OR8** | Reserved | | Disable XTAL | TE Mode Enable | Master Mode Enable | FIX Enable | NT Terminal Mode Enable | Sleep Enable |
| **OR9** | | | | | | Force INFO 2 Transmission | T3F8 Enable | T3F6 Disable |
| **OR15** | Overlay Register Enable | | Rev 5 | Rev 4 | Rev 3 | Rev 2 | Rev 1 | Rev 0 |

**Table 10–2. Overlay Register Initialization After Any Reset**

| | IDL TE | IDL NT | GCI TE | GCI NT |
|---|---|---|---|---|
| **OR0** | 00 | 00 | 00 | 00 |
| **OR1** | 04 | 04 | 00 | 00 |
| **OR2** | 08 | 08 | 00 | 00 |
| **OR3** | 00 | 00 | 00 | 00 |
| **OR4** | 04 | 04 | 00 | 00 |
| **OR5** | 08 | 08 | 00 | 00 |
| **OR6** | 00 | 00 | 00 | 00 |
| **OR7** | 00 | 00 | 00 | 00 |
| **OR8** | 00 | 00 | 00 | 01 |
| **OR15** | 00XX XXXX | 00XX XXXX | 00XX XXXX | 00XX XXXX |

NOTES:
1. All values in hexadecimal unless shown otherwise.
2. BR15 and OR15 are the same register.

## 10.2 OR0

| | (7) | (6) | (5) | (4) | (3) | (2) | (1) | (0) |
|---|---|---|---|---|---|---|---|---|
| **OR0** | $D_{in}$ B1 Channel Timeslot Bits (7:0) | | | | | | | |

**OR0(7:0) — Tx B1 Channel Timeslot**

This register allows the B1 channel timeslot input to the $D_{in}$ pin to be allocated 1 of 256 start points, corresponding to each 2–bit boundary defined by the CLK. The timeslot can be either 8 or 10 CLKs wide. The default value for OR0 is 00H.

## 10.3 OR1

| | (7) | (6) | (5) | (4) | (3) | (2) | (1) | (0) |
|---|---|---|---|---|---|---|---|---|
| **OR1** | $D_{in}$ B2 Channel Timeslot Bits (7:0) | | | | | | | |

**OR1(7:0) — Tx B2 Channel Timeslot**

This register allows the B2 channel timeslot input to the $D_{in}$ pin to be allocated 1 of 256 start points, corresponding to each 2–bit boundary defined by the CLK. The timeslot can be either 8 or 10 CLKs wide. The default value for OR1 is 04H.

## 10.4 OR2

| | (7) | (6) | (5) | (4) | (3) | (2) | (1) | (0) |
|---|---|---|---|---|---|---|---|---|
| **OR2** | $D_{in}$ D Channel Timeslot Bits (7:0) | | | | | | | |

**OR2(7:0) — Tx D Channel Timeslot**

This register allows the D channel timeslot input to the $D_{in}$ pin to be allocated 1 of 256 start points, corresponding to each 2–bit boundary defined by the CLK. The default value for OR2 is 08H.

## 10.5 OR3

| | (7) | (6) | (5) | (4) | (3) | (2) | (1) | (0) |
|---|---|---|---|---|---|---|---|---|
| **OR3** | $D_{out}$ B1 Channel Timeslot Bits (7:0) | | | | | | | |

**OR3(7:0) — Rx B1 Channel Timeslot**

This register allows the B1 channel timeslot output from the $D_{out}$ pin to be allocated 1 of 256 start points, corresponding to each 2–bit boundary defined by the CLK. The timeslot can be either 8 or 10 CLKs wide. The default value for OR3 is 00H.

## 10.6 OR4

| | (7) | (6) | (5) | (4) | (3) | (2) | (1) | (0) |
|---|---|---|---|---|---|---|---|---|
| **OR4** | $D_{out}$ B2 Channel Timeslot Bits (7:0) | | | | | | | |

**OR4(7:0) — Rx B2 Channel Timeslot**

This register allows the B2 channel timeslot output from the $D_{out}$ pin to be allocated 1 of 256 start points, corresponding to each 2–bit boundary defined by the CLK. The timeslot can be either 8 or 10 CLKs wide. The default value for OR4 is 04H.

## 10.7 OR5

| | (7) | (6) | (5) | (4) | (3) | (2) | (1) | (0) |
|---|---|---|---|---|---|---|---|---|
| **OR5** | $D_{out}$ D Channel Timeslot Bits (7:0) | | | | | | | |
| **OR5** | (GCI Indirect Mode) | | | | | S2 | S1 | S0 |

**OR5(7:0) — Rx D Channel Timeslot**

This register allows the D channel timeslot output from the $D_{out}$ pin to be allocated 1 of 256 start points, corresponding to each 2–bit boundary defined by the CLK. The default value for OR5 is 08H.

**OR5(2:0) — GCI Timeslot, S(2:0)**

In GCI indirect mode, control of the GCI timeslot is available through the S(2:0) bits. S(2:0)=0H is the initialized state, timeslot 0. The timeslot selected must be compatible with the GCI DCL clock rate being used; i.e., if the clock rate is 2048 kHz, only the first four timeslots are available. Bits 7:3 must be programmed as 0.

**Table 10–3. S(2:0) GCI Timeslot Assignment**

| S2 | S1 | S0 | Timeslot |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 2 |
| 0 | 1 | 1 | 3 |
| 1 | 0 | 0 | 4 |
| 1 | 0 | 1 | 5 |
| 1 | 1 | 0 | 6 |
| 1 | 1 | 1 | 7 |

## 10.8 OR6

| | (7) | (6) | (5) | (4) | (3) | (2) | (1) | (0) |
|---|---|---|---|---|---|---|---|---|
| **OR6** | TSA B1 Enable | TSA B2 Enable | TSA D Channel Enable | | $D_{out}$ Open Drain | GCI Indirect Mode Enable | CLK1 | CLK0 |

**OR6(7) — Control Register, TSA B1 Enable**

This bit is used to enable the B1 channel in IDL2 timeslot mode. The B1 timeslot is defined through the OR0 and OR3 registers. Whenever any channel (B1, B2, or D) is enabled for timeslot mode, all channels enter timeslot mode. If in timeslot mode and TSA B1 enable is a 0, then the B1 channel is not present on $D_{out}$, and the transmit data on the S/T interface is forced to all 1s and $D_{out}$ is high impedance.

**OR6(6) — Control Register, TSA B2 Enable**

This bit is used to enable the B2 channel in IDL2 timeslot mode. The B2 timeslot is defined through OR1 and OR4 registers. Whenever any channel (B1, B2, or D) is enabled for timeslot mode, all channels enter timeslot mode. If in timeslot mode and TSA B2 enable is a 0, then the B2 channel is not present on $D_{out}$, and the transmit data on the S/T interface is forced to all 1s and $D_{out}$ is high impedance.

**OR6(5) — Control Register, TSA D Channel Enable**

This bit is used to enable the D channel in IDL2 timeslot mode. The D timeslot is defined through the OR2 and OR5 registers. Whenever any channel (B1, B2, or D) is enabled for timeslot mode, all channels enter timeslot mode. If in timeslot mode and TSA D enable is a 0, then the D channel is not present on $D_{out}$, and the transmit data on the S/T interface is forced to all 1s and $D_{out}$ is high impedance.

**OR6(3) — Control Register, $D_{out}$ Open Drain**

When operating in NT Terminal mode, this bit configures the $D_{out}$ pin as an open drain when set to a 1. When this bit is set to a 0, the $D_{out}$ pin goes high impedance between B and D channels.

**OR6(2) — Control Register, GCI Indirect Mode Enable**

When the device is initialized, this bit is a logic 0, the inactive state; i.e., normal IDL2 mode. When set to a logic 1, the IDL2 port is reconfigured to behave like a GCI frame. This is called GCI indirect mode. When GCI indirect mode has been enabled, the GCI timeslot can be selected through the S(2:0) bits in OR5.

**OR6(1:0) — Control Register, CLK(1:0)**

In GCI indirect mode, these two bits control the output clock frequency of GCI DCL. CLK(1:0)=0H is the initialized state.

**Table 10–4. S(2:0) GCI Timeslot Assignment**

| CLK1 | CLK0 | GCI DCL |
|---|---|---|
| 0 | 0 | 2.048 MHz |
| 0 | 1 | 2.048 MHz |
| 1 | 0 | 1.536 MHz |
| 1 | 1 | 512 kHz |

## 10.9 OR7

| | (7) | (6) | (5) | (4) | (3) | (2) | (1) | (0) |
|---|---|---|---|---|---|---|---|---|
| **OR7** | Disable 3 V Regulator | Enable S/G Bit | Enable TCLK | Dual Frame Syncs | Long Frame | 8/10 Bit Select | $\overline{\text{TSEN}}$ B1/B2 Enable, BCL Enable | $\overline{\text{TSEN}}$ D Channel Enable |

**OR7(7) — Control Register, Disable 3 V Regulator**

This bit can be used to disable the supply regulator and allow three volts to be driven from an external supply. This bit is reset to a logic 0 by $\overline{\text{RESET}}$ and software reset.

**OR7(6) — Enable S/G Bit**

This bit can be enabled only in GCI 1.536 MHz clock mode. This bit provides the availability of the D channel on the S/T loop. 1 = Stop (no availability of the D channel), and 0 = Go (availability of the D channel). Refer to Section 11.2.5.

**OR7(5) — Control Register, Enable TCLK**

This is available in TE IDL2 slave mode to enable TCLK instead of TFSC. Both TFSC and TCLK are synchronized to the received S/T frames and can be used as a source of network synchronization for the slave device. Refer to the section on slave–slave mode for further details.

**OR7(4) — Control Register, Dual Frame Syncs**

This bit controls whether the IDL2 operates with one– or two–frame syncs. When set to a logic 0, the device operates with one–frame sync, and the FSC is the sync for both the Tx and Rx directions. When this bit is set to a logic 1, the FST pin is activated to be the Tx frame sync, and the FSC pin becomes the FSR (Rx frame sync). These pins will be either an input or an output depending on whether the IDL2 is a master or a slave. This bit is only functional in IDL2 mode. If dual frame syncs are enabled, then $\overline{\text{TSEN}}$ cannot be enabled.

**OR7(3) — Control Register, Long Frame**

This bit controls whether the FSC operates in long or short frame mode, while operating as an IDL2 master. If this bit is set to a 1, then the IDL2 is in long frame mode. As an IDL2 slave, the MC145574 determines the mode, based on the length of the FS. The length of the long frame is eight bit clocks, regardless of whether 8– or 10–bit format is selected. The long frame sync cannot be used in conjunction with timeslot assignment.

**OR7(2) — Control Register, 8/10 Bit Select**

When the device is initialized, this bit is a logic 0. When set to a logic 0, the IDL2 will use the 10–bit format. When set to a logic 1, the IDL2 will use the 8–bit format. When IDL2 timeslot assigner mode is enabled, the 8–bit mode is set and this bit has no effect.

**OR7(1) — Control Register, $\overline{\text{TSEN}}$ B1/B2 Enable (IDL2), BCL Enable (GCI)**

After any reset, this bit is a 0. This bit controls the operation of the $\overline{\text{TSEN}}$/BCL pin.

IDL2: $\overline{\text{TSEN}}$ B1/B2 Enable. When this bit is set to a 1, the $\overline{\text{TSEN}}$ pin function is enabled during the B1 and B2 bit times. The signal goes low when B1 or B2 data is present on $D_{out}$. This signal can be used to control a bus or backplane driver. Dual frame syncs cannot be enabled when this bit is set to a 1.

GCI: BCL Enable. When this bit is set to a 1, the BCL pin function (the 1/2 DCL clock rate signal) is enabled. Dual frame syncs cannot be enabled when this bit is set to a 1.

**OR7(0) — Control Register, $\overline{\text{TSEN}}$ D Channel Enable**

When the device is initialized, this bit is logic 0. When set to a logic 1, the $\overline{\text{TSEN}}$ signal goes low when D channel data is being output on $D_{out}$. This bit is only functional in IDL2 mode. If $\overline{\text{TSEN}}$ is

enabled, dual frame syncs cannot be enabled. $\overline{\text{TSEN}}$ D channel signal can be enabled only if $\overline{\text{TSEN}}$ B1/B2 channel signals are enabled (OR7(1) = 1).

## 10.10 OR8

| | (7) | (6) | (5) | (4) | (3) | (2) | (1) | (0) |
|---|---|---|---|---|---|---|---|---|
| **OR8** | Reserved | Reserved | Disable XTAL | TE Mode Enable | Master Mode Enable | FIX Enable | NT Terminal Mode Enable | Sleep Enable |

**OR8(7) — Reserved**
This bit is reserved.

**OR8(6) — Reserved**
This bit is reserved.

**OR8(5) — Disable XTAL**
When an external 15.36 MHz is provided, this bit can be set to 1 to disable the internal crystal buffer, thereby reducing unnecessary power consumption.

**OR8(4) — Control Register, TE Mode Enable**
When the device is initialized, this bit is a logic 0. When set to a logic 0, the device operates as normal in all modes. This bit is OR'd with the TE/$\overline{\text{NT}}$ pin and TE mode can be selected by setting this bit to a 1.

**OR8(3) — Control Register, Master Mode Enable**
When the device is initialized, this bit is a logic 0. When set to a logic 0, the device operates as normal in all modes. This bit is OR'd with the M/$\overline{\text{S}}$ pin and the NT master bit, BR7(3), and master mode can be selected by setting this bit to a 1.

**OR8(2) — Control Register, FIX Enable**
When the device is initialized, this bit is a logic 0. When set to a logic 0, the device operates as normal in all modes. In all NT modes except NT Terminal, the FIX register bit is OR'd with the FIX pin. In NT Terminal mode, the FIX bit completely replaces the function of the FIX pin. Fixed timing mode can be selected in NT mode by setting this bit to a 1.

**OR8(1) — Control Register, NT Terminal Mode Enable**
When the device is initialized, this bit is a logic 0. When set to a logic 0, the device operates as normal in all modes. NT Terminal mode can be enabled by setting this bit to 1. This bit only functions when the device is in NT mode. NT Terminal mode allows the device to have a D channel terminal port enabled. Refer to the section on NT Terminal mode.

**OR8(0) — Control Register, Sleep Enable**
When the device is initialized, this bit is a logic 0. When set to a logic 0, the device operates as normal in all modes. Please refer to the section on power modes for further operational details.

## 10.11 OR9

| | (7) | (6) | (5) | (4) | (3) | (2) | (1) | (0) |
|---|---|---|---|---|---|---|---|---|
| **OR9** | | | | | | Force INFO2 Trans–mission | T3F8 Enable | T3F6 Disable |

**OR9(2) — Control Register, Force INFO 2 Transmission**

When the device is initialized, this bit is logic 0. When set to a logic 0, the device operates as normal in all modes. This register bit is only operational in NT modes. In NT modes, the FI2 (force INFO 2 transmission) allows the software to force an activated NT (state G3) to transmit INFO 2 and reconfirm synchronization with the received INFO 3; i.e., the NT makes a G3 to G2 state jump, and on attaining G2 the FI2 bit is automatically reset. The NT then reconfirms INFO 3 and returns to the G3 state.

**OR9(1) — Control Register, T3F8 Enable**

When the device is initialized, this bit is a logic 0. When set to a logic 0, the device operates as normal in all modes. This bit only operates in the TE mode. By setting this bit to 1, the T3EXP control bit in NR2(1) is allowed to operate in F8. Hence, when in F8 and T3 expires, the device can be forced to go to the F3 state. This is in accordance with the ETSI ETS 300012 S/T–interface specification.

**OR9(0) — Control Register, T3F6 Disable**

When the device is initialized, this bit is logic 0. When set to a logic 0, the device operates as normal in all modes. This bit only operates in the TE mode. By setting this bit to a 1, the T3EXP control bit in NR2(1) is disabled from operating in F6. Hence, when in F6 and T3 expires, the device will not be forced to go to the F3 state, but will stay in F6 and transition to F7 when INFO 4 is confirmed. This is in accordance with the ETSI ETS 300012 S/T–interface specification.

## 10.12 OR15

| | (7) | (6) | (5) | (4) | (3) | (2) | (1) | (0) |
|---|---|---|---|---|---|---|---|---|
| **OR15** | Overlay Register Enable | | Rev 5 | Rev 4 | Rev 3 | Rev 2 | Rev 1 | Rev 0 |

**OR15(7) — Overlay Register Enable**

When set to a logic 1, the second set of overlay registers is enabled. The overlay register map allows access to the TSA registers required by the IDL2 and also to a GCI control register.

**OR15(5:0) — Device Revision Identification, Rev (5:0)**

The Rev (5:0) bits indicate the revision status of the device. These bits are read only and can only be modified by altering the device masks. Rev (5:0) is set to 11H for G20R1 mask set, and 03H for F57J4 mask set.

# 11
# D CHANNEL OPERATION

## 11.1 INTRODUCTION

The S/T–interface is designed for full–duplex transmission of two 64 kbps B channels and one 16 kbps D channel between one NT device and one or more TEs. The TEs gain access to the B channels by sending layer 2 frames to the network over the D channel. CCITT I.430, ETSI ETS 300012, and ANSI T1.605 specify a D channel access algorithm for TEs to gain access to the D channel. The MC145574 S/T transceiver is fully compliant with the D channel access algorithm as defined in CCITT I.430, ETSI ETS 300012, and ANSI T1.605. The D channel operation is handled through the SCP when using the S/T–interface either in IDL2 or GCI indirect mode, and handled through the C/I channel when using the S/T–interface GCI direct mode.

The various bits and pins directly pertaining to D channel operation are shown in Tables 11–1 and 11–2.

**Table 11–1. Channel SCP Bit Description**

| NT Mode | | TE Mode | |
|---|---|---|---|
| **SCP Bit** | **Description** | **SCP Bit** | **Description** |
| NR2(0) | NT Terminal Class | NR2(0) | Class |
| NR3(0) | Interrupt on D Channel Collision in NT Terminal Mode | NR3(1) | Interrupt on D Channel Collision |
| NR4(0) | Interrupt Enable for NR3(0) | NR4(1) | Interrupt Enable for NR3(1) |
| BR7(4) | Invert the Echo Channel | BR7(1) | LAPD Polarity Control |
| BR13(2) | Force the Echo Channel to 0 | BR4(4) | Map Echo Bits to D Timeslots on IDL2 Tx |
| BR13(7) | NT1 Star Mode Enable | BR7(6) | D Channel Procedures Ignored |
| OR8(1) | NT Terminal Mode Enable | | |

**Table 11–2. D Channel Operation Pin Description**

| Pin | | IDL2 Mode | GCI Mode |
|---|---|---|---|
| TQFP Pin 5 | SOIC Pin 8 | DGRANT/ANDOUT | GCI_SG/ANDOUT |
| TQFP Pin 6 | SOIC Pin 9 | DREQUEST/ANDIN | Tie Low/DREQUEST/ANDIN |
| TQFP Pin 7 | SOIC Pin 10 | CLASS/ECHO IN | Tie Low/CLASS/ECHO IN |

D channel data is clocked into the MC145574 via $D_{in}$ on the falling edges of DCL. Data is clocked out onto $D_{out}$ on the rising edges of DCL. For a detailed description of the above pins, refer to Section 7. For a detailed description of the above SCP bits, refer to Sections 8 and 9.

## 11.2 IDL2 D CHANNEL OPERATION

### 11.2.1 Gaining Access to the D Channel in the TE Mode

The pins DREQUEST and DGRANT are used in the TE mode of operation to request and grant access to the D channel. An external device wishing to send a layer 2 frame should bring DREQUEST high, and maintain it high for the duration of the layer 2 frame. DGRANT is an output signal used to indicate to an external device that the D channel is clear. Note that the DGRANT signal actually goes high one received E echo bit prior to the programmed priority class selection. DGRANT goes high at a count of (n – 1) to accommodate the delay between the input of D channel data via the IDL2 interface and the line transmission of those bits towards the NT. If at the time of the IDL2 SYNC pulse falling edge, the DGRANT and the DREQUEST signals are both detected high, the TE mode transceiver will begin FIFO buffering of the input D channel bits from the IDL2 interface. This FIFO is four bits deep. Note that DGRANT goes high on the boundaries of the demodulated E bits. In order for the contention algorithm to work on the D channel, HDLC data must be used. The MC145574 modulates the D channel data onto the S/T bus in the form that it is received from the IDL2 bus. Thus, the data must be presented to it in HDLC format. Note that one of the applications of the MC145488 DDLC is for use with the MC145574 in the terminal mode. The MC145488 performs the HDLC conversion and D channel handshaking.

### 11.2.2 Setting the Class for TE Mode of Operation

Recommendation CCITT I.430, ETSI ETS 300012, and ANSI T1.605 specifications mandate two classes of operation for a TE, with respect to D channel operation. These two classes of operation are class 1 and class 2. Each of these classes has two associated priorities; high priority and low priority. These classes and their associated priorities pertain to the number of demodulated E bits required to be 1, before the D channel is deemed to be clear for use. Using the MC145574 in the TE mode of operation, the user programs the device for class 1 or class 2 operation by either NR2(0) or Pin 10.

Table 11–3 illustrates how to configure the MC145574 for either class 1 or class 2 operation. This table also illustrates when DGRANT will go high. Note that although DGRANT goes high one E bit before the required count, data will not be modulated onto the D bit timeslots in the S/T frame until the required number of E bits = 1 are received. Thus, data gets modulated onto the D channel if the E bit following the low–to–high transition of DGRANT is 1.

**Table 11–3. MC145574 Class Operations**

| | MC145574 | Number of E Bits = 1 Required for DGRANT to Go High |
|---|---|---|
| Class 1 | NR2(0) = 0 and Pin 10 = 0 | DGRANT goes high after seven E bits = 1 in high priority, and after eight in low priority |
| Class 2 | NR2(0) = 1 or Pin 10 = 1 | DGRANT goes high after nine E bits = 1 in high priority, and after ten in low priority |

The device automatically switches from high to low priority and back, within each class of operation, in accordance with CCITT I.430, ETSI ETS 300012, and ANSI T1.605.

### 11.2.3 Generation of an Interrupt in the TE Mode

The MC145574 in the TE mode of operation generates an interrupt every time a collision occurs on the D channel. CCITT I.430, ETSI ETS 300012, and ANSI T1.605 define a collision as having occurred when the demodulated E bit from the NT does not match the previously modulated D bit from the TE. Since the NT reflects back its received D data in the E echo channel, the TE knows that a collision occurring indicates that another TE has gained access to the D channel. When a collision occurs NR3(1) gets set. If the corresponding interrupt enable bit (NR4(1)) is set high, then $\overline{IRQ}$ goes low. The D channel collision interrupt is cleared by writing a 0 to NR3(1).

### 11.2.4 Gaining Access to the D Channel in the NT Mode

When configured as an NT, the MC145574 has automatic access to the D channel. This is because the S/T–interface is designed for communication between a single NT and one or more TEs. As such, the NT does not have to compete for access to the D channel. Thus, there are no DREQUEST or DGRANT functions associated with the NT mode of operation.

Data present in the D bit positions of the IDL2 frame on IDL2 Rx are modulated onto the D bit timeslots on the S/T loop. Demodulated D channel data from the TE(s) is transmitted onto IDL2 Tx in accordance with the IDL2 specification.

The ECHO function of an NT–configured S/T transceiver is performed internally in the MC145574. To assist in testing an S/T loop, the MC145574 features the SCP test bits BR7(4) and BR13(2). Setting BR7(4) in the NT mode inverts the E echo channel (i.e., the logical inverse of the demodulated D channel data from the TE(s) is transmitted in the E channel). Setting BR13(2) to a 1 forces the E channel to all 0s. Refer to Section 9 for a more detailed description of these test bits. Setting BR13(7) to a 1 puts the NT–configured MC145574 S/T transceiver into the NT1 Star mode of operation. In this mode, the bits to be ECHOed back to the TE(s) are obtained from the ECHO IN pin. Refer to Section 13 for a more detailed description of this function.

The active polarity of the DREQUEST and DGRANT signals may be reversed by setting the LAPD polarity control bit (BR7(1)) in the SCP. When BR7(1) is a 0, the active polarity is as described above. Conversely, when BR7(1) is a 1, the MC145574 will drive DGRANT to a logic 0 when DGRANT is active, and to a logic 1 when DGRANT is inactive. Also, when BR7(1) is 1, DREQUEST will be considered to be active low.

### 11.2.5 GCI D Channel Operation

In GCI indirect mode, the D channel operation is identical to that of the IDL2.

In GCI direct mode, the DREQUEST/DGRANT/CLASS pins are replaced by C/I commands. D channel availability is indicated by two methods using the SG nomenclature; SG meaning stop/go. The stop/go refers to the availability of the D channel on the S/T loop. (1 = Stop and 0 = Go.)

The stop/go signal is available in two forms. In SCIT terminal mode, the stop/go bit is output by the device in CH2 bit 4 of the C/I channel. This method is compatible with the IOM–2 terminal mode and is also compatible with the MC68302. This mode must be enabled by selecting GCI_M(2:0) = 4H (terminal mode) and writing to OR7(6) (S/G bit enable).

The stop/go signal is also available as a pin, SG, as an alternative to the SCIT terminal method.

The SCIT terminal frame structure for the T2 device is as follows.

- The remaining CH1 and CH2 channels are for use by other devices in the terminal application, and do not form part of this specification.
- The class of message is selected using the C/I commands AR8 and AR10.
- AREOM can be used to terminate the D channel message.

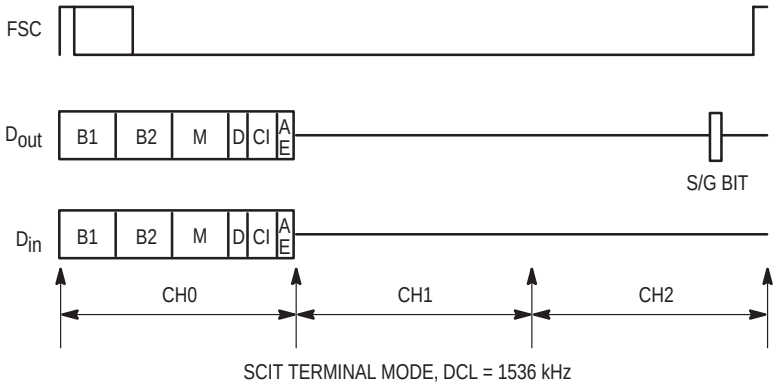



**Figure 11–1. SCIT Terminal Mode**

# 12
# MULTIFRAMING

## 12.1 INTRODUCTION

A layer 1 signalling channel between the NT and TE is provided in the MC145574 in accordance with CCITT I.430, ETSI ETS 300012, and ANSI T1.605. In the NT and TE direction, this layer 1 channel is the S channel. In the TE to NT direction, it is the Q channel. The S channel is subdivided into five subchannels: SC1, SC2, SC3, SC4, and SC5. In normal operation, the NT sets its Fa bit (Bit 14) to a binary 0 every frame. The “wrapping” action of the TE(s), as outlined in CCITT I.430, ETSI ETS 300012, and ANSI T1.605, causes the Fa bit of the TE(s) to be a 0 also. This is to ensure the existence of two line code violations per frame, enabling fast synchronization.

Multiframing is activated by the NT by setting the M bit (Bit 26) in the NT and TE frame to a binary 1, once every 20 frames. In addition to this, the Fa bit (Bit 14) in the NT to TE direction is set to a binary 1, once every five frames. When multiframing is enabled, the NT sends its S channel data (SC1 through SC5) in the S timeslot (Bit 37) every frame. Table 10–1 shows the order in which the S channel data is transmitted. Note that the M bit = 1 sets the multiframe boundary. Once every five frames, the Fa bit is set to 1 in the NT to TE direction. This serves as a Q bit identifier for the TE(s), who send their Q data in their Fa bit position in the corresponding frames. In order to avoid Q data collision, those TEs who have not been addressed for multiframing must send 1s in the Q bit timeslots.

## 12.2 ACTIVATION/DETECTION OF MULTIFRAMING IN THE MC145574

Multiframing is initiated by the NT. Detection and compliance with the multiframe structure is mandatory in the TE(s), and is automatic in the MC145574. BR7(5) is set to 1 to initiate multiframing in an NT–configured MC145574. This causes the M bit to be set to 1 in the next frame. Henceforth, the M, S, and Fa bits will automatically comply with the structure as outlined in CCITT I.430, ETSI ETS 300012, and ANSI T1.605. This format is as shown in Table 12–1. When the TE–configured MC145574 has detected multiframing, it sets NR1(1) (multiframing detect). Henceforth, it automatically complies with the multiframe format.

## 12.3 WRITING S CHANNEL DATA TO AN NT-CONFIGURED MC145574

Data written to BR2(7:4), BR9(7:4), BR9(3:0), BR10(7:4), and BR10(3:0) is transmitted in subchannels SC1, SC2, SC3, SC4, and SC5, respectively. The NT–configured MC145574 polls these internal registers once every 5 ms (a multiframe is 5 ms in duration). If no new data has been written to these registers, the old data is re–transmitted. When multiframing is disabled, the data in these registers is ignored and the Fa bit is 0. Note that in the NT mode, these registers come out of reset in the all–0s state.

**Table 12–1. S Channel Data Transmission**

| Frame No. | NT to TE Fa Bit Position | NT to TE M Bit | NT to TE S Bit | TE to NT Fa Bit Position |
|---|---|---|---|---|
| 1 | 1 | 1 | SC1.1 | Q1 |
| 2 | 0 | 0 | SC2.1 | 0 |
| 3 | 0 | 0 | SC3.1 | 0 |
| 4 | 0 | 0 | SC4.1 | 0 |
| 5 | 0 | 0 | SC5.1 | 0 |
| 6 | 1 | 0 | SC1.2 | Q2 |
| 7 | 0 | 0 | SC2.2 | 0 |
| 8 | 0 | 0 | SC3.2 | 0 |
| 9 | 0 | 0 | SC4.2 | 0 |
| 10 | 0 | 0 | SC5.2 | 0 |
| 11 | 1 | 0 | SC1.3 | Q3 |
| 12 | 0 | 0 | SC2.3 | 0 |
| 13 | 0 | 0 | SC3.3 | 0 |
| 14 | 0 | 0 | SC4.3 | 0 |
| 15 | 0 | 0 | SC5.3 | 0 |
| 16 | 1 | 0 | SC1.4 | Q4 |
| 17 | 0 | 0 | SC2.4 | 0 |
| 18 | 0 | 0 | SC3.4 | 0 |
| 19 | 0 | 0 | SC4.4 | 0 |
| 20 | 0 | 0 | SC5.4 | 0 |
| 1 | 1 | 1 | SC1.1 | Q1 |
| 2 | 0 | 0 | SC2.1 | 0 |

## 12.4 MULTIFRAME INTERRUPTS IN AN NT-CONFIGURED MC145574

The NT will generate an interrupt either once every multiframe, or only in the event of a new Q channel nibble having been received. A new Q channel nibble is defined as one which differs from the previous Q nibble.

Table 12–2 illustrates how to configure an NT for either of these options.

**Table 12–2. Multiframe Interrupts**

| BR3(2) Interrupt Every Multiframe | NR4(2) Enable Multiframing Interrupt | IRQ MC145574 |
|---|---|---|
| X | 0 | Multiframing never causes an interrupt |
| 0 | 1 | An interrupt is generated on the reception of a new Q Channel nibble |
| 1 | 1 | An interrupt is generated every multiframe |

## 12.5 READING Q CHANNEL DATA FROM AN NT-CONFIGURED MC145574

The Q data nibble received from the TE(s) is obtained by reading BR3(7:4). The demodulated Q channel data is written to this register every 5 ms. BR3(7:4) are read only bits.

## 12.6 WRITING Q CHANNEL DATA TO A TE-CONFIGURED MC145574

Data written to BR2(7:4) is transmitted in the Q channel. The TE–configured MC145574 polls this internal register once every 5 ms (a multiframe is 5 ms in duration). If no new data has been written to this register, the old data is re–transmitted. When multiframing is disabled, the data in this register is ignored and the Fa bit obeys the multiframing wrapping criteria as outlined in CCITT I.430, ETSI ETS 300012, and ANSI T1.605.

BR2(7:4) comes out of reset in the all–1s state in the TE mode of operation. To accommodate other TEs on the loop, BR2(7:4) should be left in the all–1s state when the TE does not have access to the Q channel.

## 12.7 MULTIFRAME INTERRUPTS IN A TE-CONFIGURED MC145574

The TE will generate an interrupt either once every multiframe or only in the event of a new SC1 subchannel nibble having been received. A new SC1 subchannel nibble is defined as one which differs from the previous SC1 nibble. Table 12–3 illustrates how to configure a TE for either of these options.

**Table 12–3. TE Multiframe Interrupts**

| BR3(2)<br>Interrupt Every<br>Multiframe | NR4(2)<br>Enable Multiframing<br>Interrupt | IRQ<br>MC145574 |
|---|---|---|
| X | 0 | Multiframing never causes an interrupt |
| 0 | 1 | An interrupt is generated on the reception of a new SC1 subchannel nibble |
| 1 | 1 | An interrupt is generated every multiframe |

## 12.8 READING S SUBCHANNEL DATA FROM A TE-CONFIGURED MC145574

The S subchannel nibbles SC1, SC2, SC3, SC4, and SC5 received from the NT are obtained by reading BR3(7:4), BR9(7:4), BR9(3:0), BR10(7:4), and BR10(3:0), respectively. The demodulated S subchannel data is written to these registers every 5 ms. These registers are read only registers in the TE mode of operation.

## 12.9 MULTIFRAMING IN GCI MODE

Multiframing can be enabled in GCI mode by writing/reading to BR7(5) via the Monitor channel.

# 13
# DEVICE CONFIGURATIONS

The MC145574 can be configured in several different modes for different applications. The following sections describe the various configurations available for the NT and TE modes.

## 13.1 NT CONFIGURATIONS

To select NT mode, the TE/$\overline{\text{NT}}$ pin must be held low. The NT device can operate in a mixture of different configurations. How each aspect of the NT's operation is selected is discussed separately in the following sections. However, for a broad view of the NT's various flavors, the NT family tree is shown in Figure 13–1.

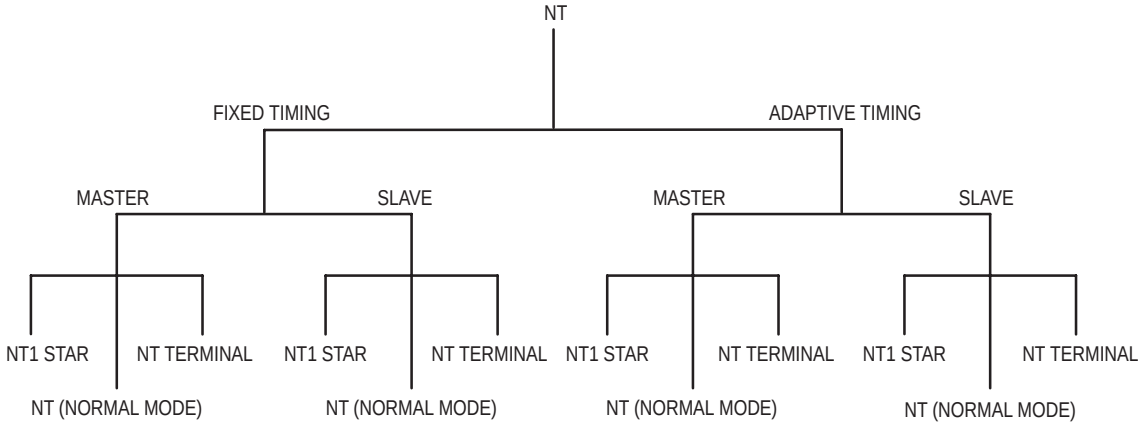



**Figure 13–1. NT Family Tree**

### 13.1.1 NT Fixed or Adaptive Timing

The receiver/demodulator of the NT can operate in two different modes depending on the type of loop that the device is connected to. These modes are called fixed and adaptive timing modes. The mode of operation is chosen by the state of Pin 6. When this pin is held low the device is in adaptive mode, and when held high the device is in fixed timing mode. The choice of mode is dependent on the loop characteristics, and the intention is that fixed timing should be used for short passive bus configurations and adaptive timing used for all others. However, the performance of the timing recovery circuit employed in the MC145474/75, and also in the MC145574, allows the use of adaptive timing in all loop configurations. Thus, it is recommended that adaptive timing be used in all configurations.

It is also possible to select fixed timing mode via the SCP/GCI control bit OR8(2). The FIX pin is internally OR'd with this SCP/GCI bit, and one should note that in the NT Terminal mode, this is the only way to select fixed timing. The FIX pin should be held low if register programming is to be used.

### 13.1.2 NT Master or Slave

In NT mode, the IDL2/GCI interface can be selected either as a master or a slave. This selection is done via Pin 5. When Pin 5 is held low, slave mode is selected. When it is held high, master mode is selected.

In slave mode, the IDL2/GCI interface frame sync and clock are inputs, and the S/T loop interface timing is slaved to these inputs. In master mode, the IDL2/GCI interface frame sync and clock are outputs; these signals being derived from the 15.36 MHz XTAL oscillator. The S/T loop interface timing, however, is always slaved to the IDL2/GCI frame sync.

Therefore, in NT mode, the S/T loop interface timing is always slaved to the IDL2/GCI frame sync. The source of this timing can be selected to be from the IDL2/GCI driver (slave mode) or from the NT device itself (master mode).

NT master mode will be referred to as NTM, and NT slave mode as NTS.

It is also possible to select NTM by writing to the SCP control bit BR7(3). Or alternatively in TE or NT mode, master selection can be made via OR8(3). The master/slave pin is internally OR'd with these SCP bits and should be held low if register is to be used.

### 13.1.3 NT1 Star and NT Terminal Modes

In NT mode, two further mode extensions can be selected via control bits accessible through the SCP. These NT mode extensions have no effect on the IDL2 interface, but alter the operation of other pins to perform the desired functions. These two modes are called NT1 Star and NT Terminal.

**Table 13–1. Pin Operations**

| Pin | | NT | NT1 Star | NT Terminal |
|---|---|---|---|---|
| TQFP Pin 3 | SOIC Pin 6 | FIX | FIX | T_IN |
| TQFP Pin 5 | SOIC Pin 8 | High–Z | ANDOUT | DGRANT |
| TQFP Pin 6 | SOIC Pin 9 | Tie–Low | ANDIN | DREQUEST |
| TQFP Pin 7 | SOIC Pin 10 | Tie–Low | ECHO IN | CLASS |

#### 13.1.3.1 NT1 Star Mode

Appendix B of ANSI T1.605 describes an example of an NT that will support multiple T interfaces. This is to accommodate multipoint operation with more than eight TEs. The MC145574 can be configured for NT1 Star mode of operation. This mode is for use in wire OR'ing multiple NT–configured S/T chips on the IDL2 side. Each NT has a common FSC, DCL, $D_{out}$, and $D_{in}$, as shown in Figure 13–2. Each NT is then connected to its own individual S/T loop containing either a single TE or a group of TEs. As such, the contention for either of the B channels or for the D channel is now extended from a single passive bus to a grouping of passive busses.

ISDN employs the use of HDLC data on the D channel. Access to either of the B channels is requested and either granted or denied by the user sending layer 2 frames on the D channel. In normal operation where there is only one NT, the TEs are granted access to the D channel in accordance with their priority and class. By counting the required number of E channel echo bits being 1, the TEs know when the D channel is clear. Thus, in the NT1 Star mode of operation, where there are multiple passive busses competing for the same B1, B2, and D channels, the same E echo channel must be transmitted from each NT to its passive bus. This is accomplished in the MC145574 by means of the ANDIN, ANDOUT, and ECHO IN pins.

Figure 13–2 shows how to connect the multiple number of NTs in the NT1 Star mode. Successive connection of the ANDOUT (this is the output of an internal AND gate whose inputs are the demodulated D bits and the data on the ANDIN pin) and ANDIN pins, and the common connections of the ECHO IN pins, succeeds in sending the same E echo channel to each group of TE(s). To configure a series of NTs for NT1 Star mode, BR13(7) must be set to 1 in each NT. Data transmitted on Tx in NT1 Star mode will have the following format: a logic 0 is $V_{SS}$; a logic 1 causes $D_{out}$ to go to a high–impedance state. This then permits the series wire OR'ing of the IDL2 bus. Note that one of the NTs must have its ANDIN pin pulled high.

NT1 Star mode is not applicable to the NT using the GCI interface.

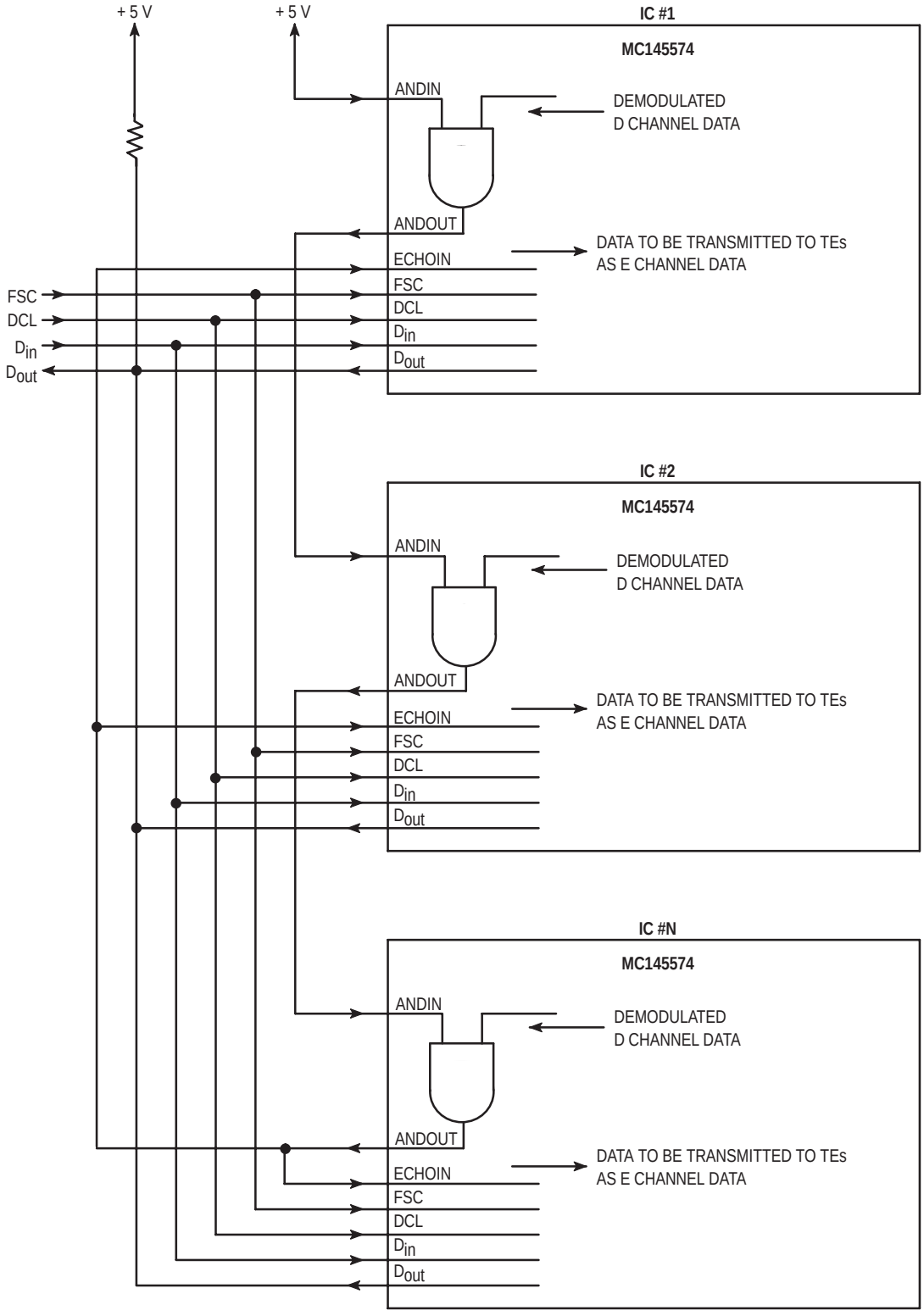



**Figure 13–2. NT1 Star Mode of Operation**

#### 13.1.3.2 NT Terminal Mode

In NT Terminal mode, another IDL2 channel data port is opened on the device. This port has four pins associated with it. They are DREQUEST, DGRANT, CLASS, and T_IN.

This port has the capability of competing for access to the D channel with the TEs connected to the passive bus. To do this, the DREQUEST, DGRANT, and CLASS functions normally associated with the TE are enabled. This allows an external controlling device to request access to the D channel, and if the D channel is idle, be given access. The NT device monitors the received S/T loop D bits to determine whether the channel is busy or not (a TE device would monitor the E bits).

Once the controlling device has been given access to the D channel, the MC145574 indicates this by setting DGRANT high and enabling the D slot on the T_IN pin.

The NT device ANDs the received D bits from the S/T loop with D channel data received from the T_IN pin, and transmits this as the E bit on the S/T loop. The AND'd data is then passed to the $D_{out}$ for output.

DGRANT is high when the S/T is not activated.

Contention is monitored by comparing the transmitted E bit to the D channel data from the T_IN pin. If they are not equal then contention from a device on the S/T loop is assumed, and the D channel access halted. An interrupt IRQ7, NR3(0), is generated to indicate contention has occurred.

The T_IN pin also accepts data on the B1 and B2 slots. This data is AND'd with the received B1 and B2 data from the S/T–interface and then output on the $D_{out}$ pin. There is no provision on the device to detect data collision on the B channels. (The B channels are enabled by default.)

The T_IN IDL2 port is synchronized to the normal IDL2 port by FSC, and the DCL clock is used to sample the T_IN pin. NT Terminal mode operates in all the IDL2 modes, including TSA and dual frame sync modes.

When the $D_{out}$ pin is configured as an open drain output, a pullup resistor (between 1 k and 10 k) is needed.

The T_IN port has the same format as the IDL2 or GCI that is being used.

Data can be input to the T_IN pin when the MC145574 is either activated or deactivated. NT Terminal mode operates when the MC145574 is either activated or deactivated.

## 13.2 TE CONFIGURATIONS

To select TE mode, Pin 4 (TE/$\overline{NT}$) must be held high, or alternatively, by writing to the SCP control bit OR8(4). This bit is internally OR'd with the TE/$\overline{NT}$ pin. In TE mode, the device operates in two different configurations, these configurations being TE slave (TES) and TE master (TEM).

The selection of slave or master is accomplished via Pin 5. When held low, slave mode is selected; and when held high, master mode is selected.

Each mode is discussed separately in the following sections; however, certain shared pins have different functions in TES and TEM mode. (See Table 13–2.)

**Table 13–2. Pin Operations for Master and Slave Modes**

| Pin | | TEM | TES |
|---|---|---|---|
| TQFP Pin 3 | SOIC Pin 6 | High–Z | TFSC/TCLK |
| TQFP Pin 5 | SOIC Pin 8 | DGRANT | High–Z |
| TQFP Pin 6 | SOIC Pin 9 | DREQUEST | Tie $V_{SS}$ |
| TQFP Pin 7 | SOIC Pin 10 | CLASS | Tie $V_{SS}$ |

There is no fixed/adaptive timing selection to be made in TE mode. In TE mode, the MC145574 always uses adaptive timing.

### 13.2.1 TE Master Mode (TEM)

The TEM mode is the normal mode of operation for a TE. The two main operational features of TEM mode are as follows.

The IDL2/GCI is a master of the digital interface. This means that the IDL2/GCI outputs the frame sync and clock. The frame sync and clock are signals derived from the received S/T loop signal (i.e., timing is recovered from the received INFO transmitted by the NT and is used to generate the IDL2 signals so the TE end can operate synchronously with the NT).

The D channel access procedure outlined in the ANSI spec is enabled. This means that access to the D channel is controlled via a set of rules designed to enable secure HDLC data transmission on a shared channel, and provides a means for the TEM to recognize when collisions have occurred. This operation is fully detailed in Section 11, D Channel Operation.

The three pins used to control the D channel access are DREQUEST, DGRANT, and CLASS.

### 13.2.2 TE Slave Mode (TES)

In TES mode, the IDL2/GCI interface operates in slave mode; i.e., the IDL2/GCI frame sync and clock are inputs. This mode is intended for use in NT2 applications where the IDL2/GCI interface timing is derived from a low jitter network synchronous source. The MC145574 has jitter/wander buffers which absorb the clock/frame sync jitter and prevent data loss. The MC145574 will be able to absorb 60 μs peak–to–peak wander, which exceeds the 18 μs peak–to–peak over 24 hours wander stated in Q.502.

There is no D channel contention circuitry in TES mode. The device has transparent access to the D channel. It is intended that the TES operates in point–to–point applications only and thus does not need D channel contention arbitration.

To facilitate the generation of the timing signals required by the slave IDL2/GCI interface, a pin is provided which outputs a frame sync or a clock. These signals are synchronized to the received INFO transmitted by the NT and can be used to provide network timing if no other source in the NT2 is available. The choice of frame sync or clock and the frequency of the clock are all selectable via the SCP.

The TFSC output is to allow the NT2 to be synchronized to the network. The TFSC is an 8 kHz frame sync signal that is synchronized to the received network signal.

Alternatively, TFSC can be reprogrammed via the SCP to provide TCLK. TCLK is a clock, whose frequency can be chosen via the SCP, which is also synchronized to the received S/T–interface. TCLK can be used as an alternative to TFSC in NT2 slave–slave mode. The frequency of TCLK is selected in the same manner as the DCL frequency is selected in the TE master mode.

In both the TFSC and TCLK cases, the output pin senses if a signal is present; and if not, the output is enabled and the device outputs its signal. This allows the TES devices to have this pin wire OR'd with only one of the active devices outputting the sync clock. For this function to work correctly, the pin must have an external resistor connected to $V_{DD}$ I/O.

| BR13(5) | BR7(2) | TCLK |
|---|---|---|
| 0 | 0 | 2.56 MHz |
| 0 | 1 | 2.048 MHz |
| 1 | 0 | 1.536 MHz |
| 1 | 1 | 512 kHz |

An example architecture of an NT2 is shown in Figure 13–3. The TFSC signal supplied by the TE in slave mode is used via a clocksource selector to synchronize the whole NT2 to the network.

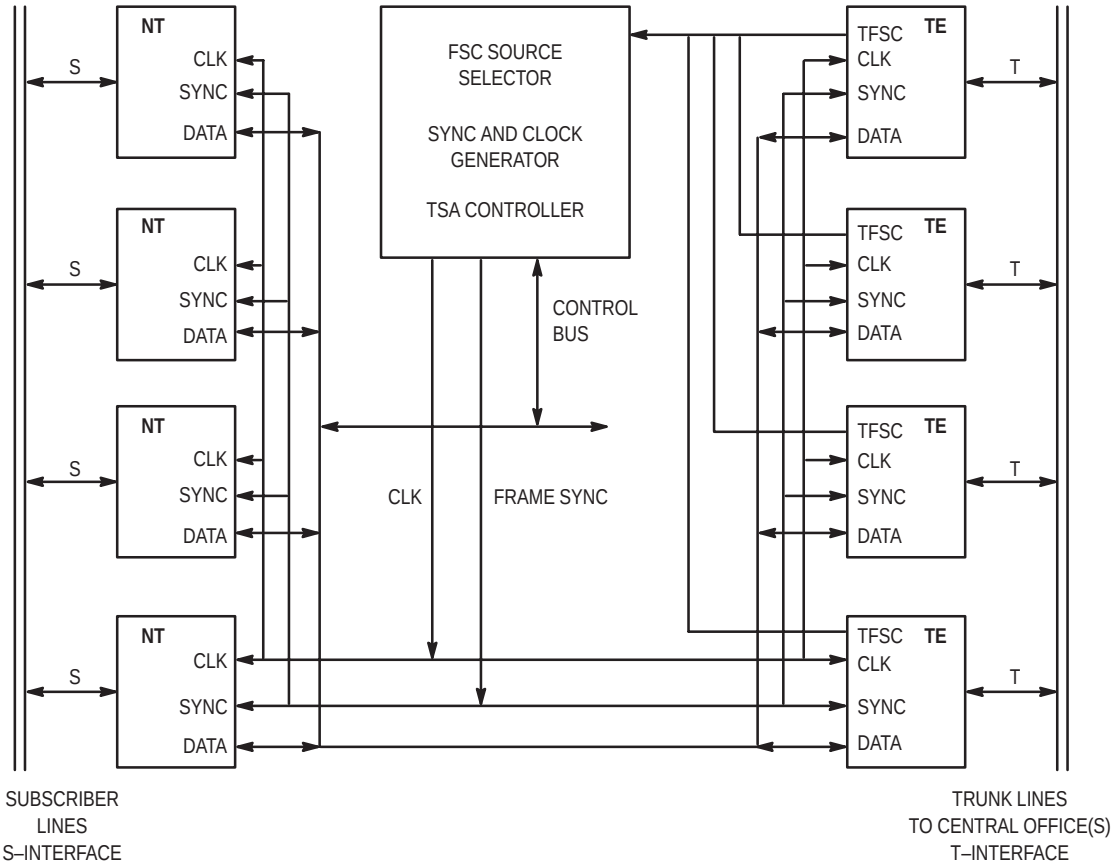



**Figure 13–3. NT2 Architecture**

# 14
# CLOCK INTERFACE

Figure 14–1 shows the recommended crystal oscillator for connection to the MC145574.

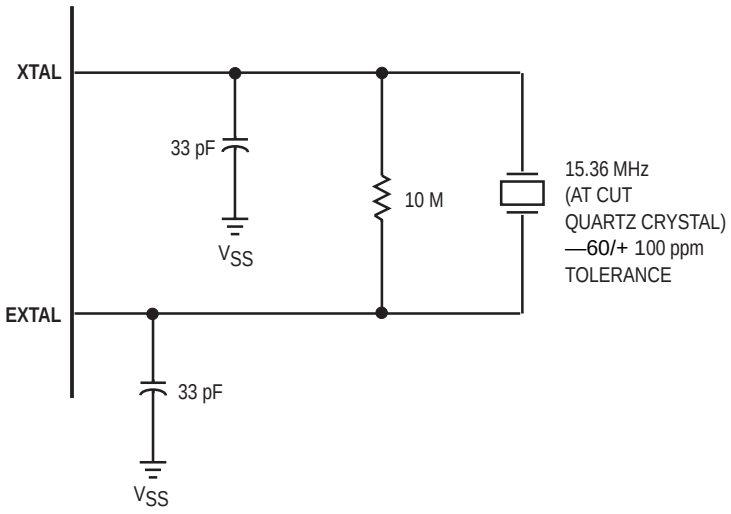



**Figure 14–1. Typical Crystal Oscillator Connection**

Figure 14–2 shows the connection when using an external clock.

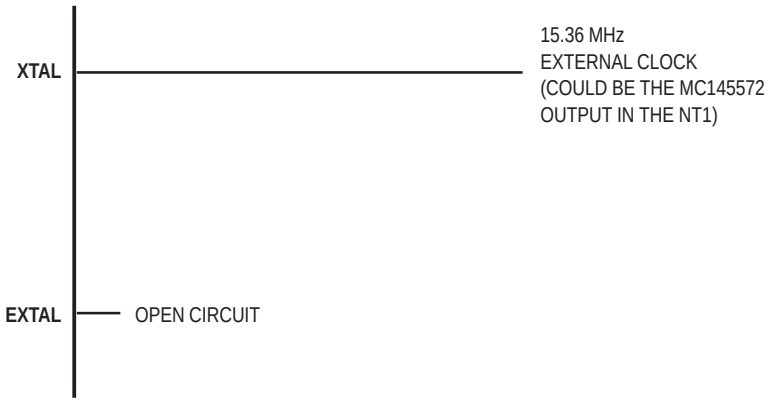



**Figure 14–2. Connection with External Clock**

# 15
# INTERRUPTS

## 15.1 INTRODUCTION

When the MC145574 in SCP is configured as a TE, it has three interrupt modes. When the MC145574 is configured as an NT, it has four interrupt modes. Each of these interrupts is maskable. When an interrupt occurs (and if the interrupt condition is enabled), the MC145574 asserts the $\overline{IRQ}$ pin. A detailed description of these interrupts, and how they are cleared, follows.

## 15.2 IRQ7 NR3(0) — NT : D CHANNEL COLLISION TE : NOT APPLICABLE NR4(0) — ENABLE

IRQ7 is used in the NT Terminal mode of the MC145574 to indicate that a collision has occurred on the D channel. This bit operates in the same manner as the IRQ1 interrupt in TE mode, and likewise is cleared by writing a 0 to the NR3(0) bit. This action also releases the $\overline{IRQ}$ pin.

Note that this bit is maskable by means of NR4(0). This interrupt is only applicable in the NT mode and is therefore not available in the TE mode.

## 15.3 IRQ1 NR3(1) — TE: D CHANNEL COLLISION NT: NOT APPLICABLE NR4(1) — ENABLE

IRQ1 is used in the TE mode of operation of the MC145574 to indicate to external devices that a collision has occurred on the D channel. A D channel collision is considered to have occurred when the TE is transmitting on the D channel (both DREQUEST and DGRANT being high) and the received E echo bit from the NT does not match the previously modulated D bit. When IRQ1 occurs, the MC145574 internally sets NR3(1) to a 1. If the IRQ1 ENABLE is set to 1, an interrupt to an external device is generated. The interrupt condition is cleared by writing a 0 to NR3(1). Note that this bit is maskable by means of NR4(1). This interrupt is only applicable in the TE mode and is therefore not available in the NT mode.

## 15.4 IRQ2 NR3(2) — MULTIFRAME RECEPTION NR4(2) — ENABLE

IRQ2 is provided for multiframing reception indication. This interrupt is applicable and available in both NT and TE modes of operation of the MC145574. Note that this interrupt is maskable by means of NR4(2). Multiframing is initiated by the NT by setting BR7(5). A multiframe is 20 basic frames, or 5 ms in duration. If this interrupt is enabled (it is enabled by setting NR4(2)) and if multiframing is in progress, then an interrupt is generated on multiframe boundaries; i.e., every 5 ms. Alternatively, an NT–configured MC145574 can be programmed to generate an interrupt only in the event of a new Q channel nibble having been received. Similarly, a TE–configured MC145574 can be programmed to generate an interrupt only in the event of a new SC1 subchannel having been received. Refer to Section 12 for a detailed description of these features.

If an interrupt is to occur, it will do so in the 47th baud of the transmitted frame of the 20th frame in a multiframe. Data to be transmitted in the SC1 through SC5 subchannels in the NT is internally latched from BR2(7:4), BR9(7:0), and BR10(7:0) during the 47th baud of the transmitted frame of the 20th frame in a multiframe. At this time, the received Q channel nibble is made available by internally

latching the data to BR3(7:4). Similarly, data to be transmitted in the Q channel of the TE is internally latched from BR2(7:4) during the 47th baud of the transmitted INFO 3 in the 20th frame of a multiframe. At this time, the received SC1 through SC5 subchannel nibbles is also made available. A mutiframing interrupt is cleared by reading BR3. Reading BR3 clears the interrupt in both the NT and TE modes of operation, regardless of whether the MC145574 is configured to generate an interrupt in the event of a new nibble or every multiframe. Note that NR3(2) is a read only bit.

## 15.5 IRQ3 NR3(3) — CHANGE IN Rx INFO STATE NR4(3) — ENABLE

IRQ3 is provided to indicate a change in the received INFO state of the transceiver. In the NT mode, this corresponds to a change in the receiving INFO 0, INFO 1, INFO 3, or INFO X state. Alternatively, in the TE mode this corresponds to a change in the receiving INFO 0, INFO 2, INFO 4, or INFO X state. Thus, when a change occurs in one of these states, the MC145574 internally sets NR3(3) to a 1. If the IRQ3 ENABLE is set to 1, an interrupt to an external device will be generated. IRQ3 can be cleared by writing a 0 to NR3(3). This bit is reset by a software reset or a hardware reset. Note that the transmission states for the NT (INFO 0, INFO 2, and INFO 4) and for the TE (INFO 0, INFO 1, and INFO 3) are as defined in Section 3. INFO X is defined as any transmission state other than those states. An example of such a state would be when the MC145574 is programmed to transmit a 96 kHz test signal (BR11(0) = 1). The MC145574 comes out of reset in the receiving “INFO X” state. Hence, IRQ3 will be generated when it recognizes either INFO 0, INFO 1, INFO 2, INFO 3, or INFO 4. Note that NR3(3) is a read/write bit.

As soon as INFO 0, INFO LOW (1 or 2), or INFO HIGH (3 or 4) is detected, an interrupt is generated. If the INFO X state persists for > 8 ms, then an INFO X interrupt is generated.

## 15.6 IRQ6 NR3(1) — NT : FAR-END CODE VIOLATION (FECV) DETECTION TE : NOT APPLICABLE NR4(1) — ENABLE

The interrupt request condition IRQ6 is generated when the NT has detected a far–end code violation (FECV). An FECV occurs when a multiframe incoming to the NT from the TE(s) contains one or more illegal S/T line code violations. This interrupt is used to indicate to an NT when to send an FECV layer 1 maintenance message to the TEs as defined in ANSI T1.605. When IRQ6 occurs, the MC145574 internally sets NR3(1) to a 1. If the IRQ6 ENABLE is set to 1, an interrupt to an external device will be generated. The interrupt condition is cleared by writing a 0 to NR3(1).

Note that this bit is maskable by means of NR4(1). This interrupt is applicable in the NT mode of operation and only when multiframing has been enabled.

## 15.7 GCI MODE

In GCI mode, a Monitor channel message is output by the MC145574 if an equivalent SCP interrupt condition has occurred. This message must be enabled by writing to the NR4 register (via the Monitor channel). The Monitor channel message that occurs in response to an interrupt condition contains the content of NR3.

# 16
# TRANSMISSION LINE INTERFACE CIRCUITRY

## 16.1 INTRODUCTION

The MC145574 is an ISDN S/T transceiver fully compliant with CCITT I.430, ETSI ETS 300012, and ANSI T1.605. As such, it is designed to interface with a four–wire transmission medium, one pair being the transmit path, the other pair the receive path. TxP and TxN, a fully–differential output transmit pair from the MC145574, are designed to interface to the transmit pair of the transmission medium via auxiliary discrete components and a 1:2.5 turns ratio transformer. RxP and RxN are a high–impedance differential input pair used for coupling the receive line signal through a 1:2.5 turns ratio transformer.

## 16.2 TRANSMIT LINE INTERFACE CIRCUITRY

The TxP and TxN pins on the MC145574 act as a current–limited differential voltage source pair. The TxP and TxN pair behave as active drivers when creating logical 0 line signals (CCITT I.430, ETSI ETS 300012, and ANSI T1.605 define the nominal pulse amplitude to be 750 mV, zero to peak, for a 50 Ω load), and are high–impedance outputs when generating logical 1 signals. The transmit circuitry within the S/T transceiver is designed to operate with a 1:2.5 turns ratio line interface transformer. The transmit transformer is similar in design to the receive transformer.

The TxP and TxN pair operate as a 2.8 V current–limited differential voltage source on the device side (1.12 V on the S/T loop side). As such, two 5% series resistors should be inserted in the line interface circuit so that the combined resistance of these two resistors and the winding resistance of the transformer is 145 Ω. The current limit value is set by circuitry within the S/T transceiver and is approximately 9 mA.

The TxP and TxN transmit pair supplies a current such that a positive potential is created between the TxP and TxN pins, respectively, when transmitting the F frame bit of each frame. The TxP and TxN line drive circuit of the MC145574 S/T transceiver is designed such that the device continues to provide a high–impedance circuit to the transmit pair of the S/T loop when power is removed (i.e., when the circuit between $V_{DD}$ and $V_{SS}$ becomes a short circuit). Figure 16–1 illustrates the recommended line interface and protection circuitry for interfacing the MC145574 to the S/T loop.

## 16.3 RECEIVE LINE INTERFACE CIRCUITRY

The RxP and RxN pins serve as a fully–differential input pair for the line signal from the S/T loop. The input impedance seen looking into the combination of the MC145574 and the associated receive line interface circuitry (as shown in Figure 16–2) exceeds the CCITT I.430, ETSI ETS 300012, and ANSI T1.605 requirements under all conditions. The receive line circuitry within the MC145574 S/T transceiver is designed to operate with a 1:2.5 turns ratio transformer. The receive transformer is similar in design to the transmit transformer and a list of suppliers of these transformers are included.

The receive circuitry within the MC145574 automatically adapts to the optimum ternary detection thresholds for receiving the incoming line signal, regardless of the S/T loop bus configuration. The minimum ternary detection threshold is 90 mV, referenced to signal ground. This value then sets the absolute maximum attenuation that can exist, before detection of the incoming signal becomes impossible. The RxP and RxN pair are not sensitive to the polarity of their connection to the line interface circuitry. Figure 16–2 illustrates the recommended line interface and protection circuitry for interfacing the MC145574 S/T transceiver to the loop.

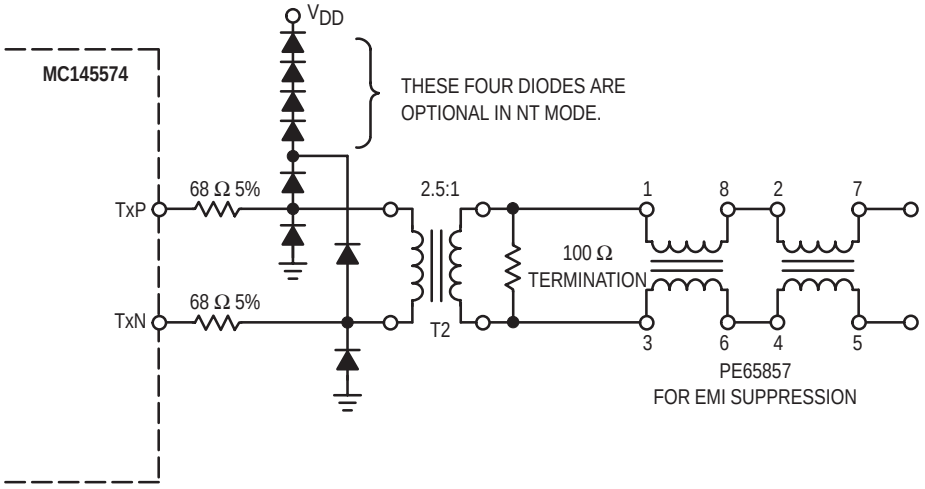
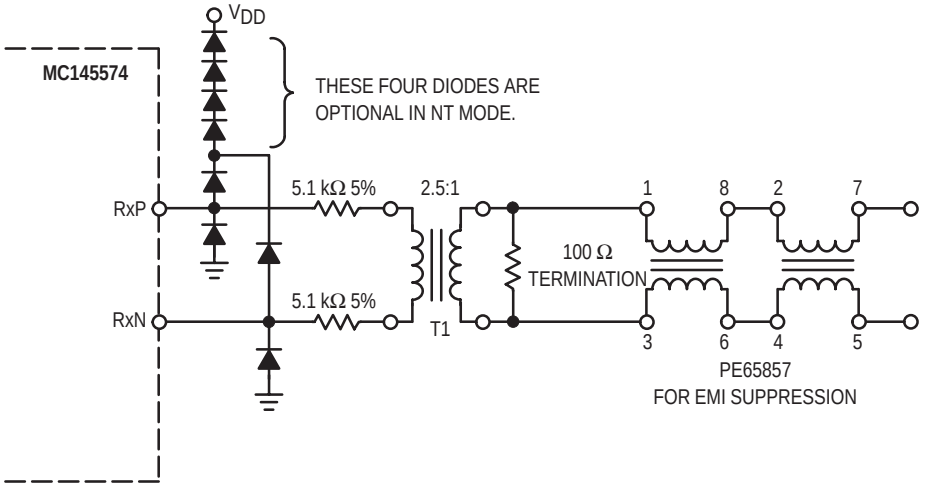



**Figure 16–1. Transmit Line Interface Circuit**




NOTES:
1. Diodes are 1N4148 or MMAD1108.
2. The MMAD1108 is a monolithic array of eight diodes and is a Motorola preferred device.
3. All resistors are 1/4 watt.

**Figure 16–2. Receive Line Interface Circuit**

## 16.4 ADDITIONAL NOTES

### 16.4.1 Sources of Line Interface Transformers

Line interface transformers for use with the MC145574 S/T may be obtained from the following manufacturers:

Pulse Engineering
P.O. Box 12235
San Diego, California 92112
Tel : 619–674–8100
Fax : 619–674–8262
Part # PE 64998 (single)
Part # PE 65498 (dual)

Secre Composants
117, rue de Cambrai
75019 Paris, France
Tel : (331) 44–89–48–00
Fax : (331) 42–05–15–19
Part # E01170, E01167
Part # E01171 (SMD)

FEE S.A.
Zone Industrielle
39270 Orgelet
France
Tel: (33) 84–35–04–04
Fax: (33) 84–25–46–41
Part # FE2150

APC
47 Riverside, Medway City Estate
Strood, Rochester, Kent ME2 4DP
United Kingdom
Tel: (44) 1634–290–588
Fax: (44) 1634–290–591
Part # APC15103

Motorola cannot recommend one manufacturer over another and in no way implies that this is a complete listing.

### 16.4.2 Termination Resistors

Note that the 100 Ω termination resistors in the transmit and receive line circuitry (as shown in Figures 16–1 and 16–2) are mandatory when operating as an NT in accordance with CCITT I.430, ETSI ETS 300012, and ANSI T1.605. When operating as a TE in point–to–point mode, these are also required. However, when configured as a TE in the passive bus arrangement, only one TE has these termination resistors. The 100 Ω termination resistor should also be removed for some conformance tests.

### 16.4.3 Protection Diodes

CCITT I.430, ETSI ETS 300012, and ANSI T1.605 specify that the S/T–interface voltage cannot exceed 1.6 times the nominal voltage of 750 mV (= 1.2 V). Since the MC145574 is designed to operate with 2.5:1 turns ratio transformers, the diode structure as illustrated in Figures 16–1 and 16–2 is required to provide protection, while not adversely affecting the S/T–interface when power is removed from the device. This diode structure also protects the circuit against electrostatic discharges (ESD) and latch–up.

**CAUTION**

The four pins RxP, RxN, TxP, and TxN are not internally protected against ESD and caution must be taken during handling and mounting the devices to prevent any possible electrical overstress.

# 17
# POWER MODE OPERATION

## 17.1 POWER SUPPLY STRATEGY

The MC145574 operates from a 5 V ± 5% supply. The MC145574 has an on–chip linear regulator. This regulator has an output of 3.2 V. This regulated 3 V supply powers all of the internal digital logic, resulting in reduced power consumption. The analog receiver/transmitter blocks are powered from the 5 V supply.

The 3 V regulated output is present on the $V_{DD}3$ pin. A capacitor of 100 nF should be connected between this pin and $V_{SS}$ to provide filtering for the internal regulator.

If a more efficient 3 V supply is available in the application circuit, then the $V_{DD}3$ pin can be driven directly with this external supply. The internal 3 V regulator should then be disabled via the SCP to gain a further improvement in device power consumption. This can be achieved by setting OR7(7).

The 5 V supply is still required when an external 3 V supply is being used.

The digital output drivers have a separate +ve supply pin, $V_{DD}$ I/O. This pin should be connected to $V_{DD}5$ if 5 V output drivers are required, or the $V_{DD}3$ pin if 3 V output drivers are required. This option allows the device to be easily interfaced to 3 V or 5 V CMOS or TTL devices. Using 3 V drivers will give reduced power consumption while still being able to interface to 3 V CMOS and TTL devices.

All the digital inputs operate from the 3 V regulated supply ($V_{DD}3$) and are TTL and CMOS compatible. The input ESD protection is connected to $V_{DD}5$ (the 5 V supply) ensuring that the inputs are compatible with 3 V or 5 V CMOS and TTL input levels.

The 15.36 MHz crystal oscillator is powered from the 3 V regulated supply ($V_{DD}3$) to minimize its power consumption. The XTAL oscillator circuit can be disabled via the SCP control bit (OR8(5)) if an external 15.36 MHz clock source is available, further improving power consumption.

## 17.2 POWER MODES

The MC145574 has four distinct modes in which the maximum power consumption of the device is specified.

### 17.2.1 Normal Operation

In this mode, the device is free to operate and activate or be activated from the S/T–interface.

In this mode, the device consumes the maximum power when it is forced to transmit the 96 kHz test signal into the correctly terminated (50 Ω) interface circuit. The receiver should also be receiving a 96 kHz test signal.

### 17.2.2 Transmit Power-Down

In this mode, the device has its transmit circuitry powered down. This is achieved by setting the NR0(2) in the SCP. The receiver is still fully active and able to respond to S/T–interface initiated activation. The power consumption is measured with RxINFO = INFO 0. This mode can be entered or exited in SCP or GCI mode.

### 17.2.3 Absolute Minimum Power

In this mode, the device is forced into the absolute minimum power state from which it cannot be activated from the S/T–interface. All internal circuits are disabled, including the XTAL oscillator, and only the SCP interface remains functional. All possible power consumption in the Tx and Rx analog circuitry is blocked.

In IDL2/SCP mode, this power mode is entered/exited by writing to the NR0(1) register in the SCP.

In GCI mode, this power reduction mode is not available.

The characteristics of this mode are identical to that in the MC145474 except for the XTAL oscillator, which is disabled in the MC145574.

### 17.2.4 Sleep

In this mode, the device is in a power conservation mode where all possible power consuming circuitry is switched off, including the XTAL OSC.

In SCP mode, the sleep mode is enabled by writing to OR8(0). When the device goes into the sleep state, only the SCP and an energy detector with receiver remain operational.

In GCI mode, the sleep mode is enabled by default. The sleep mode can be disabled by writing the OR8(0) via the Monitor channel. When the device goes into the sleep state, only the GCI interface and an energy detector in the receiver remains operational. Sleep mode is not available with NT master GCI/SCP configuration.

In both SCP and GCI modes, the device will enter the sleep state (assuming sleep mode is enabled) when the MC145574 detects no activity on the S/T–interface and is in the deactivated state. A timer is then enabled which will cause the MC145574 to enter the sleep state after a period of 2 ms.

The sleep state is exited when a signal is detected on the S/T–interface. In this case, the device exits sleep mode and tries to synchronize to the signal. If successful, the device activates in the normal function. The sleep state can also be exited by writing an activate request via the SCP. This cause the device to exit the sleep state and attempt to activate in the normal function.

In GCI slave mode, the sleep state is exited by using the AR command on the C/I channel.

In GCI master mode (TE master only), the sleep mode is exited by first pulling the $D_{in}$ pin low to request that the GCI clock starts, and then issuing the TIM command (if only the GCI interface is to be activated), or by issuing the AR command if an activation is to be attempted.

When the MC145574 enters the sleep state, the crystal oscillator is disabled, i.e., stopped.

# 18
# ELECTRICAL SPECIFICATIONS

## 18.1 MAXIMUM RATINGS

This device contains circuitry to protect the inputs against damage due to high static voltages or electrical fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, it is recommended that $V_{in}$ and $V_{out}$ be constrained in the range $V_{SS} \le (V_{in}$ or $V_{out}) \ge V_{DD}5$. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage (e.g., either $V_{SS}$ or $V_{DD}5$). All of the reliability data and the ESD results are available on request from your local sales office or your nearest distributor.

**MAXIMUM RATINGS** (Voltages Referenced to $V_{SS}$)

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}5$ | Supply Voltage | – 0.5 to + 7 | V |
| $V_{in}$ | Input Voltage (Any Pin to $V_{SS}$) | – 0.3 to $V_{DD}5$ + 0.3 | V |
| I | DC Current (Any Pin Excluding $V_{DD}5$, $V_{DD}$ I/O, $V_{DD}3$, $V_{SS}$, TxP, and TxN) | ± 10 | mA |
| $T_A$ | Operating Temperature Range | – 40 to + 85 | °C |
| $T_{stg}$ | Storage Temperature Range | – 85 to + 150 | °C |

NOTE: Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description section.

## 18.2 DIGITAL DC ELECTRICAL CHARACTERISTICS

($T_A$ = – 40 to + 85°C, $V_{DD}5$ = 5.0 V ± 5%, Voltages Referenced to $V_{SS}$)

| Characteristic | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Input High Voltage | $V_{IH}$ | 2.0 | — | V |
| Input Low Voltage | $V_{IL}$ | — | 0.8 | V |
| Input Leakage Current @ 5.25 V | $I_{in}$ | — | 5 | µA |
| High Impedance Input Current @ 4.5/0.5 V | Ilkg(Z) | — | 10 | µA |
| Input Capacitance | $C_{in}$ | — | 10 | pF |
| Output High Voltage ($I_{OH}$ = – 400 µA) | $V_{OH}$ | 2.4 | — | V |
| Output Low Voltage ($I_{OL}$ = 5.0 mA) | $V_{OL}$ | — | 0.4 | V |
| XTAL Input High level | $V_{IH(X)}$ | 3.0 | — | V |
| XTAL Input Low level | $V_{IL(X)}$ | — | 0.5 | V |
| EXTAL Output Current ($V_{OH}$ = 4.6 V) | $I_{OH(X)}$ | — | – 400 | µA |
| EXTAL Output Current ($V_{OL}$ = 0.4 V) | $I_{OL(X)}$ | — | 400 | µA |
| IRQ Output Low Current ($V_{OL}$ = 0.4 V) | | — | 2 | mA |
| IRQ Output Off State Impedance | | 100 | — | kΩ |

## 18.3 ANALOG CHARACTERISTICS

($T_A$ = – 40 to + 85°C, $V_{DD}$ = 5.0 V ± 5%, Voltages Referenced to $V_{SS}$)

| Characteristic | Min | Typ | Max | Unit |
|---|---|---|---|---|
| TxP/TxN Drive Current: $R_L$ = 50 Ω | 5.4 | 6.0 | 6.6 | mA |
| (TxP – TxN) Voltage Limit | — | — | 1.17 | Vpeak |
| Rx Input Sensitivity, Normal Mode (RxP – RxN) | 90 | — | — | mVpeak |
| Rx Input Sensitivity, Sleep Mode (RxP – RxN) | 220 | — | — | mVpeak |
| Voltage Regulator | 3.0 | 3.2 | 3.4 | V |

## 18.4 POWER DISSIPATION

($T_A$ = – 40 to + 85°C, $V_{DD}$ = 5.0 V ± 5%, Voltages Referenced to $V_{SS}$ and $V_{DD}$ I/O Connected to $V_{DD}$)

| Characteristic | Min | Typ | Max | Unit |
|---|---|---|---|---|
| DC Supply Voltage | 4.75 | 5 | 5.25 | V |
| Worst Case Power Consumption** | — | 60* | 90 | mW |
| Transmit Power Down | — | 50* | 70 | mW |
| Sleep Mode | — | 0.5* | 4 | mW |
| Absolute Minimum Power Down | — | 0.1* | 2 | mW |

NOTES:

* These values have been measured on some sampled devices from several lots at 25°C and 5 V $V_{DD}$.

** While sending and receiving 96 kHz signal on S/T–interface.

## 18.5 IDL2 TIMING CHARACTERISTICS

### 18.5.1 IDL2 Master Timing, 8- and 10-Bit Formats

| Ref. No. | Parameter | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|
| 1 | FSC Period | 125 | 125 | — | µs | 1 |
| 2 | Delay From the Rising Edge of DCL to the Rising Edge of FSC | — | — | 30 | ns | |
| 3 | Delay From the Rising Edge of DCL to the Falling Edge of FSC | — | — | 30 | ns | |
| 4 | DCL Clock Period | 391 | — | 1953 | ns | 2 |
| 5 | DCL Pulse Width High, Nominal 512 kHz<br>1.536 MHz<br>2.048 MHz<br>2.56 MHz | 878<br>293<br>220<br>175 | —<br>—<br>—<br>— | 1074<br>358<br>265<br>215 | ns | 3 |
| 6 | DCL Pulse Width Low | 45 | — | 55 | % of DCL Period | |
| 7 | Delay From Rising Edge of DCL to Low–Z and Valid Data on $D_{out}$ | — | — | 30 | ns | |
| 8 | Delay From Rising Edge of DCL to Data Valid on $D_{out}$ | 5 | — | 30 | ns | |
| 9 | Delay From Rising Edge of DCL to High–Z on $D_{out}$ | — | — | 30 | ns | |
| 10 | Data Valid on $D_{in}$ Before Falling Edge of DCL ($D_{in}$ Setup Time) | 25 | — | — | ns | |
| 11 | Data Valid on $D_{in}$ After Falling Edge of DCL ($D_{in}$ Hold Time) | 25 | — | — | ns | |
| 12 | Delay From Rising Edge of DCL to $\overline{TSEN}$ Low | — | — | 30 | ns | 4 |
| 13 | Delay From Falling Edge of DCL to $\overline{TSEN}$ High | — | — | 30 | ns | |

NOTES:
1. FSC occurs on average every 125 µs.
2. The DCL frequency may be 512 kHz, 1.536 MHz, 2.048 MHz, or 2.56 MHz.
3. The duty cycle of DCL is between 45% and 55% when operated in Master Timing mode.
4. In IDL 8– and 10–bit formats, $\overline{TSEN}$ can be valid during the B1, B2, and D channel timeslots.

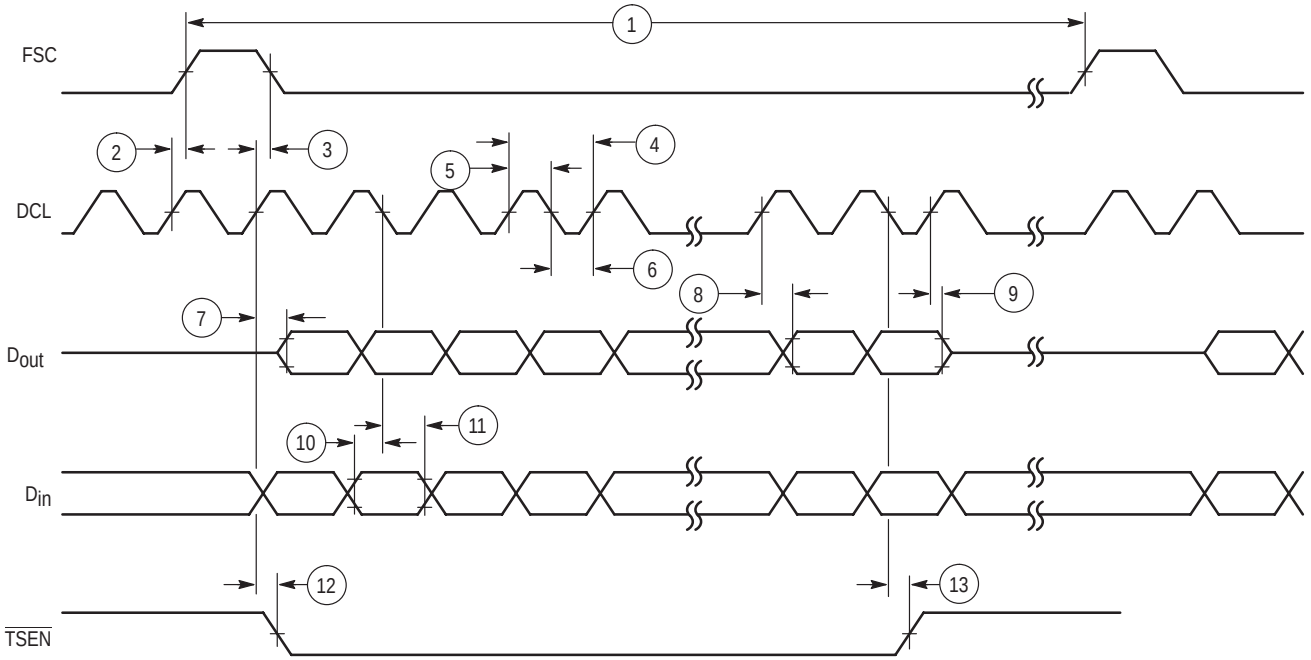



**Figure 18–1. IDL2 Master Timing, 8– and 10–Bit Formats**

## 18.5.2 IDL2 Slave Timing, 8- and 10-Bit Formats

| Ref. No. | Parameter | Min | Max | Unit | Note |
|---|---|---|---|---|---|
| 14 | FSC Period | 125 | — | µs | 1 |
| 15 | FSC High Before the Falling Edge of DCL (FSC Setup Time) | 25 | — | ns | |
| 16 | FSC High After the Falling Edge of DCL (FSC Hold Time) | 25 | — | ns | |
| 17 | Delay From Rising Edge of DCL to Low–Z and Valid Data on $D_{out}$ | — | 30 | ns | |
| 18 | Delay From Rising Edge of DCL to Data Valid on $D_{out}$ | — | 30 | ns | |
| 19 | Delay From Rising Edge of DCL to High–Z on $D_{out}$ | 5 | 30 | ns | |
| 20 | Delay From Rising Edge of DCL to $\overline{TSEN}$ Low | — | 30 | ns | 2 |
| 21 | Delay From Rising Edge of DCL to $\overline{TSEN}$ High | — | 30 | ns | |
| 22 | DCL Clock Period | 244 | 1953 | ns | 3 |
| 23 | DCL Pulse Width High | 45 | 55 | % of DCL Period | |
| 24 | DCL Pulse Width Low | 45 | 55 | % of DCL Period | |
| 25 | Data Valid on $D_{in}$ Before Falling Edge of DCL ($D_{in}$ Setup Time) | 25 | — | ns | |
| 26 | Data Valid on $D_{in}$ After Falling Edge of DCL ($D_{in}$ Hold Time) | 25 | — | ns | |

NOTES:

1. FSC occurs on average every 125 µs. FSC must occur every 125 µs with a maximum instantaneous phase titter of ± 30 µs.
2. In IDL2 8– and 10–bit formats, $\overline{TSEN}$ is valid during the B1, B2, and D channel timeslots. $\overline{TSEN}$ will be aligned with data on the $D_{out}$ pin.
3. In IDL2 Slave mode, DCL may be any frequency multiple of 8 kHz between 256 kHz and 4.096 MHz inclusive.

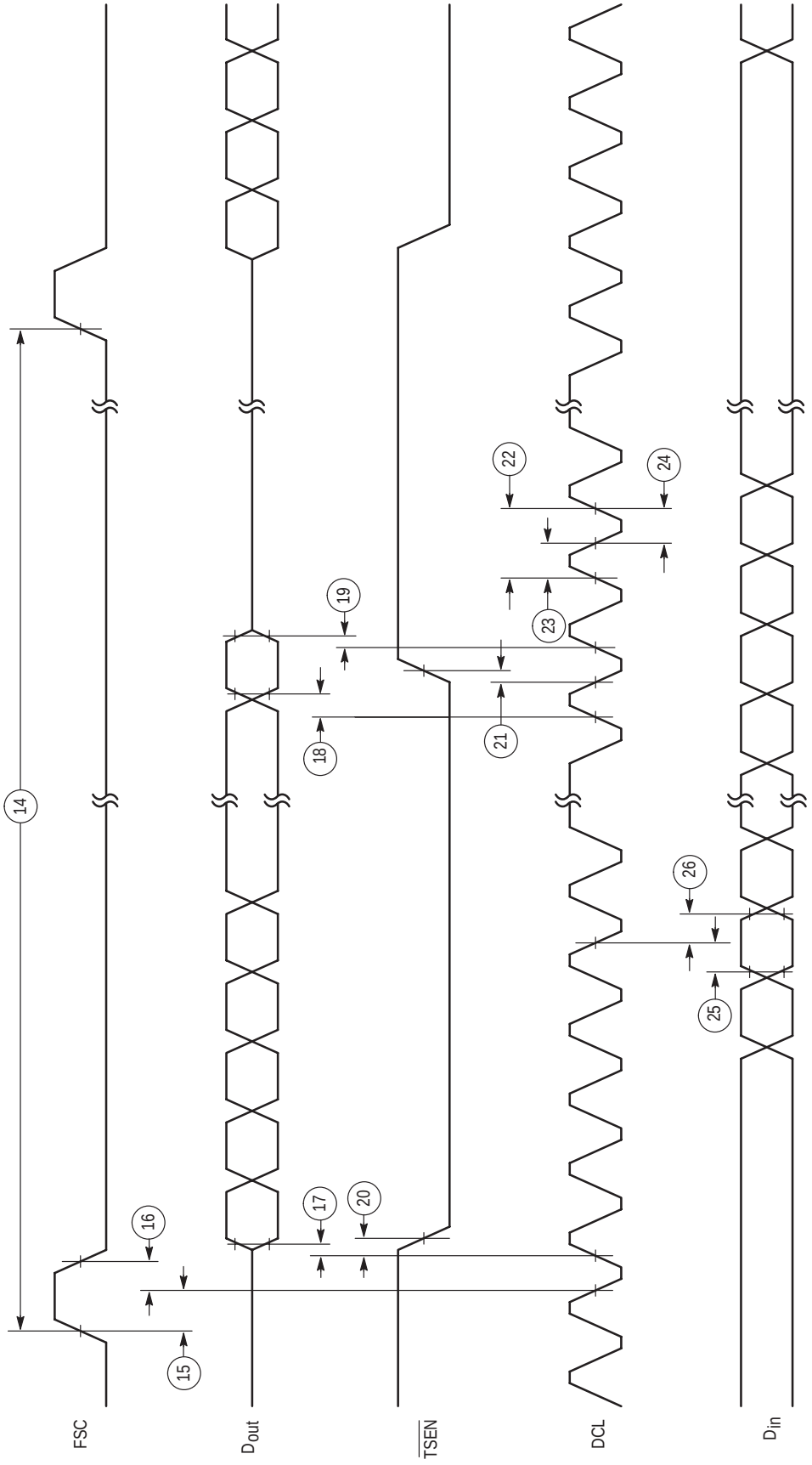



**Figure 18–2. IDL2 Slave Timing, 8– and 10–Bit Formats**

## 18.6 GCI TIMING FOR MASTER AND SLAVE MODE

| Ref. No. | Parameter | Min | Max | Unit | Note |
|---|---|---|---|---|---|
| 1 | Delay From Rising Edge of DCL to FSC Output High | — | 30 | ns | |
| 2 | Delay From Rising Edge of DCL to FSC Output Low | — | 30 | ns | 1 |
| 3 | FSC Input High Before the Falling Edge of DCL (FSC Setup Time) | 25 | — | ns | |
| 4 | FSC Input High After the Falling Edge of FSC (FSC Hold Time) | 25 | — | ns | |
| 5a | DCL Clock Period Master Mode | 488 | 1953 | ns | 2 |
| 5b | DCL Clock Period Slave Mode | 244 | 1953 | ns | 3 |
| 6 | DCL Pulse Width High 512 kHz<br>2.048 kHz | 878<br>210 | 1074<br>265 | ns | 4 |
| 7 | DCL Pulse Width Low | 45 | 55 | % of DCL Period | |
| 8 | DCL Fall Time | 5 | 15 | ns | |
| 9 | DCL Rise Time | 5 | 15 | ns | |
| 10 | Delay From Rising Edge of FSC to Low–Z and Valid Data on $D_{out}$ | — | 30 | ns | |
| 11 | Delay From Rising Edge of DCL to Data Valid on $D_{out}$ | — | 30 | ns | |
| 12 | Delay From Rising Edge of DCL High–Z on $D_{out}$ | 5 | 30 | ns | |
| 13 | Data Valid on $D_{in}$ Before Rising Edge of DCL | 25 | — | ns | |
| 14 | Data Valid on $D_{in}$ After Rising Edge of DCL | 25 | — | ns | |
| 15 | Delay From Rising Edge of FSC to $\overline{TSEN}$ Low | — | 30 | ns | |
| 16 | Delay From Rising Edge of DCL to $\overline{TSEN}$ High | — | 30 | ns | |

NOTES:
1. The FSC pulse is normally two DCL clock periods wide in GCI mode.
2. In GCI Master mode, the MC145574 will output a 512 kHz, 1.536 MHz or 2.048 MHz clock as selected by M2, M1 and M0 pins.
3. In GCI Slave mode, DCL may be any frequency that is a multiple of 512 kHz and is between 512 kHz and 4.096 MHz.
4. The duty cycle of DCL is between 45% and 55% when operated in Master Timing mode.

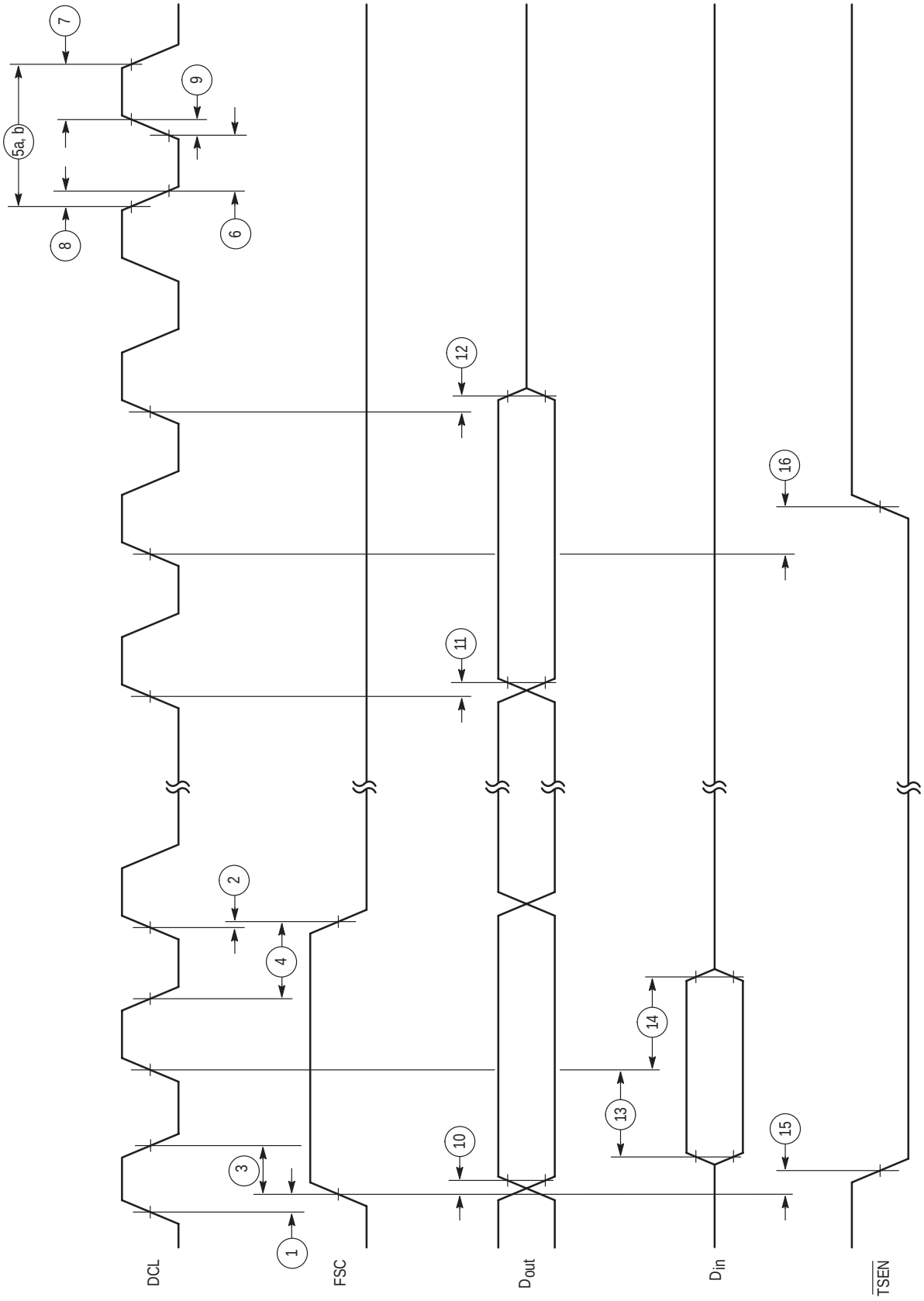


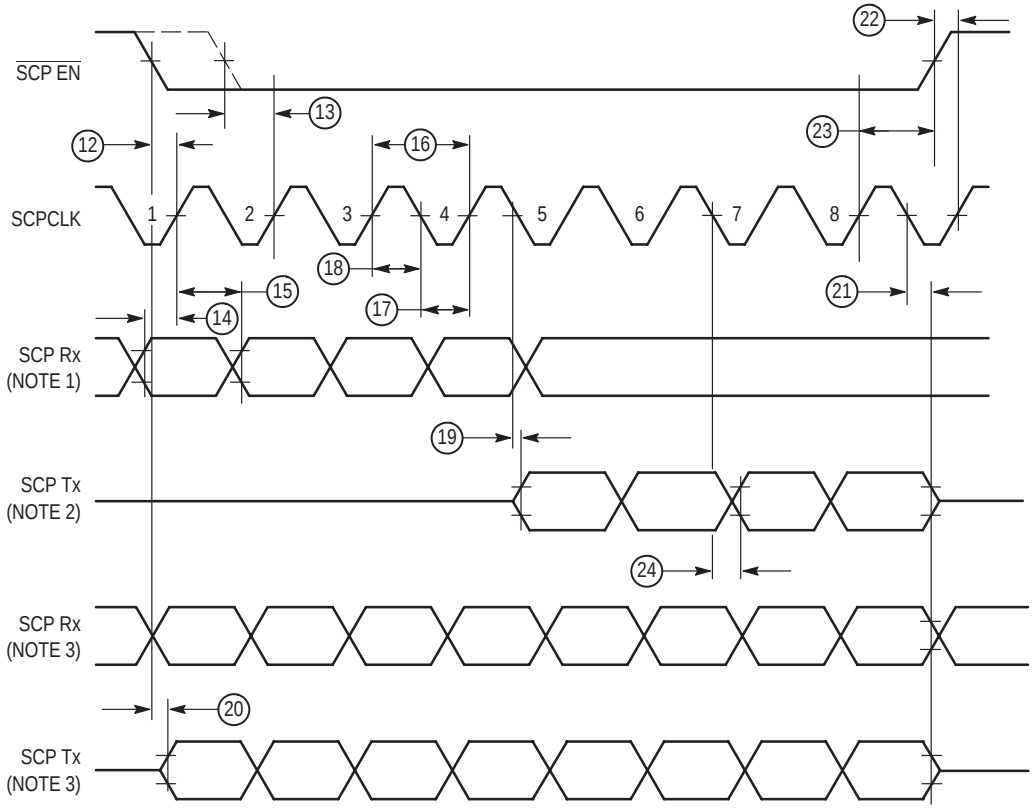

**Figure 18–3. GCI Timing For Master and Slave Mode**

## 18.7 SCP TIMING CHARACTERISTICS

($T_A$ = – 40 to + 85°C, $V_{DD}$ = 5.0 V ± 5%, Voltages Referenced to $V_{SS}$)

| Ref. No. | Characteristic | Min | Max | Unit |
|---|---|---|---|---|
| 12 | $\overline{\text{SCPEN}}$ Active Before Rising Edge of SCPCLK | 50 | — | ns |
| 13 | SCP Rising Edge Before $\overline{\text{SCPEN}}$ Active | 50 | — | ns |
| 14 | SCP Rx Valid Before SCPCLK Rising Edge (Setup Time) | 20 | — | ns |
| 15 | SCP Rx Valid After SCPCLK Rising Edge (Hold Time) | 20 | — | ns |
| 16 | SCPCLK Period (Note 1) | 244 | — | ns |
| 17 | SCPCLK Width (Low) | 30 | — | ns |
| 18 | SCPCLK Width (High) | 30 | — | ns |
| 19 | SCP Tx Active Delay | — | 50 | ns |
| 20 | $\overline{\text{SCPEN}}$ Active to SCP Tx Active | — | 50 | ns |
| 21 | SCPCLK Falling Edge to SCP Tx High–Impedance | — | 40 | ns |
| 22 | $\overline{\text{SCPEN}}$ Inactive Before SCPCLK Rising Edge | 50 | — | ns |
| 23 | SCPCLK Rising Edge Before $\overline{\text{SCPEN}}$ Inactive | 50 | — | ns |
| 24 | SCPCLK Falling Edge to SCP Tx Valid Data | — | 50 | ns |

NOTE:
1. Maximum SCP Clock Frequency is 4.096 MHz.




NOTES:
1. During a nibble read, four bits are presented on SCP Rx.
2. During a nibble read, SCP Tx will be active for the duration of the 4–bit transmission as shown.
3. During a byte read, eight bits are presented on SCP Rx. A byte transaction consists of two 8–bit exchanges. During the second 8–bit exchange, data is either written to the byte from SCP Rx or is read from the byte. If the operation is a read operation, then data is presented onto SCP Tx. Refer to Section 5, “The Serial Control Port”, for a detailed description.

**Figure 18–4. SCP Timing Characteristics**

## 18.8 NT1 STAR MODE TIMING CHARACTERISTICS

| Ref. No. | Characteristic | Min | Max | Unit |
|---|---|---|---|---|
| 25 | Propagation Delay from ANDIN to ANDOUT | — | 35 | ns |

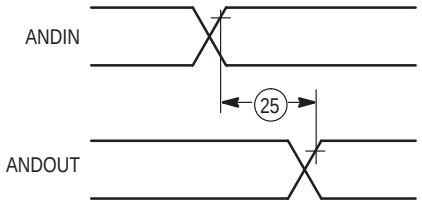



**Figure 18–5. NT1 Star Mode**

## 18.9 D CHANNEL TIMING CHARACTERISTICS (IDL2 MODE)

| Ref. No. | Characteristic | Min | Max | Unit |
|---|---|---|---|---|
| 26 | DREQUEST Valid Before Falling Edge of FSC | 30 | — | ns |
| 27 | DREQUEST Valid After Falling Edge of FSC | 30 | — | ns |
| 28 | DGRANT Valid Before Falling Edge of FSC | 390 | — | ns |

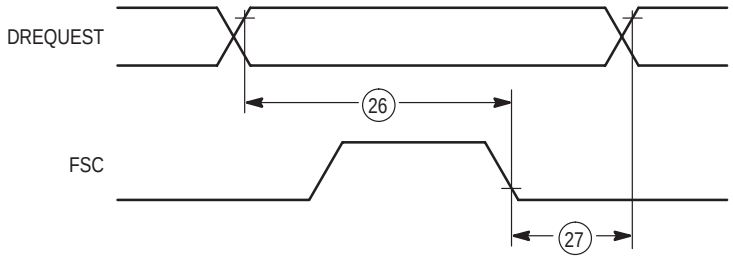



**Figure 18–6. D Channel Request Timing**

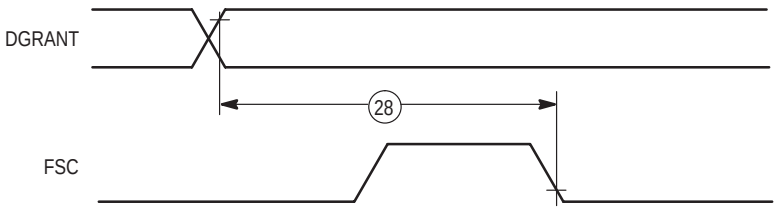



**Figure 18–7. D Channel Grant Timing**

# 19
# MECHANICAL DATA

## 19.1 PIN ASSIGNMENTS

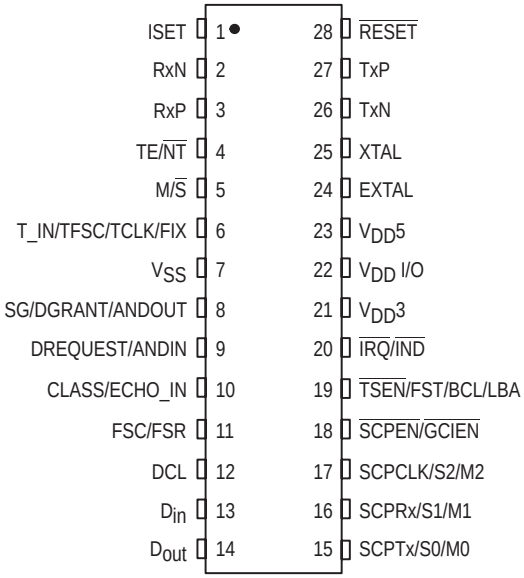



**Figure 19–1. MC145574DW Pin Assignment (SOIC 28–Pin Package, Case 751F)**

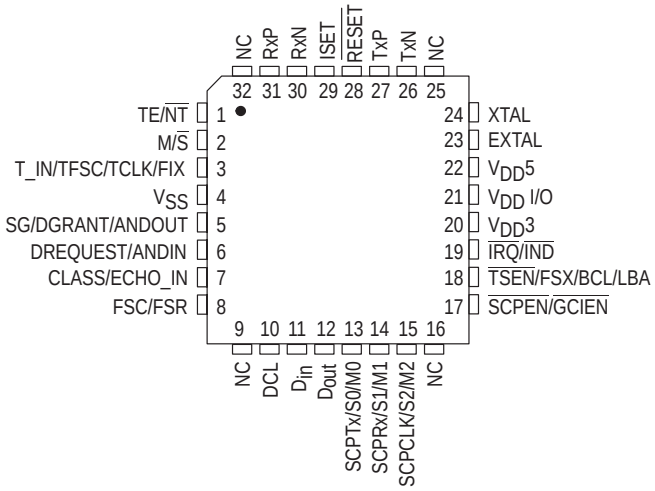
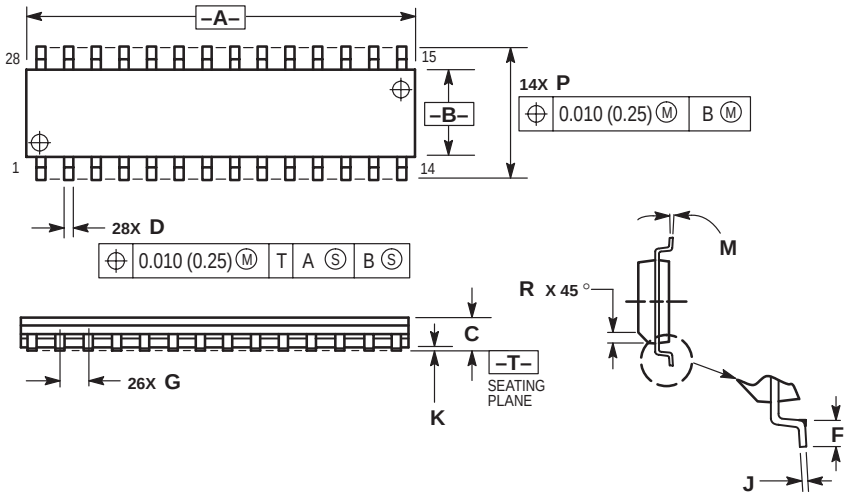



**Figure 19–2. MC145574PB Pin Assignment (TQFP 32–Pin Package, Case 873A)**

## 19.2 PACKAGE DIMENSIONS

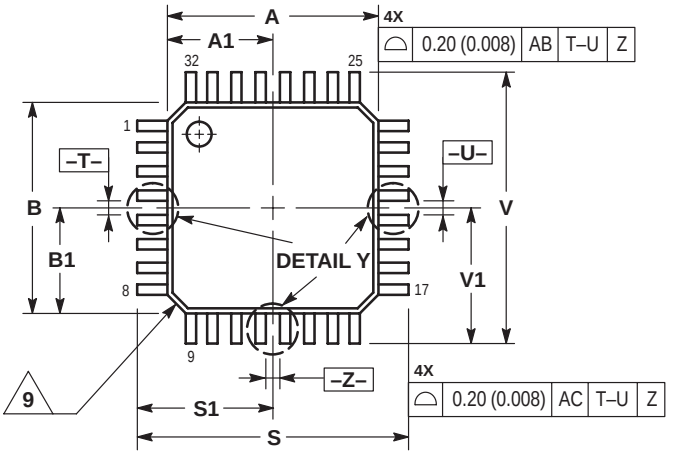
**DW SUFFIX**
**SOIC**
**CASE 751F–04**

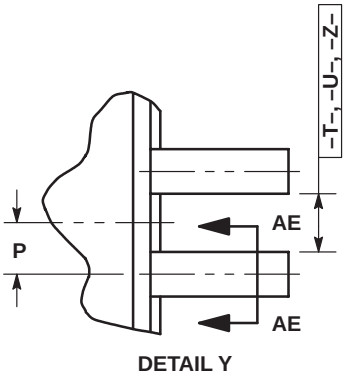



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

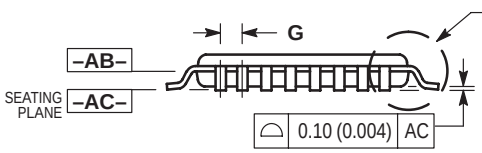
| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 17.80 | 18.05 | 0.701 | 0.711 |
| B | 7.40 | 7.60 | 0.292 | 0.299 |
| C | 2.35 | 2.65 | 0.093 | 0.104 |
| D | 0.35 | 0.49 | 0.014 | 0.019 |
| F | 0.41 | 0.90 | 0.016 | 0.035 |
| G | 1.27 BSC | | 0.050 BSC | |
| J | 0.23 | 0.32 | 0.009 | 0.013 |
| K | 0.13 | 0.29 | 0.005 | 0.011 |
| M | 0 ° | 8 ° | 0 ° | 8 ° |
| P | 10.01 | 10.55 | 0.395 | 0.415 |
| R | 0.25 | 0.75 | 0.010 | 0.029 |

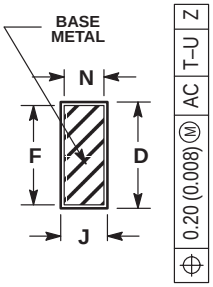
**PB SUFFIX**
**TQFP**
**CASE 873A–02**



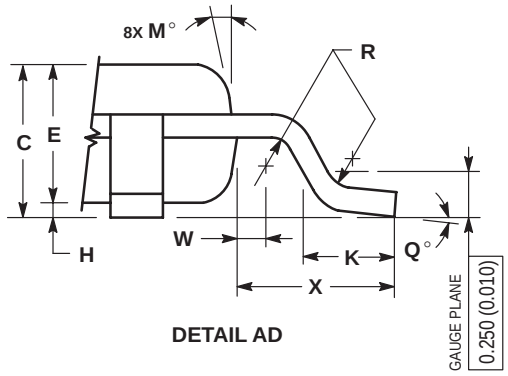




**DETAIL Y**




**SECTION AE–AE**




**DETAIL AD**

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE –AB– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS –T–, –U–, AND –Z– TO BE DETERMINED AT DATUM PLANE –AB–.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE –AC–.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –AB–.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.520 (0.020).
8. MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076 (0.0003).
9. EXACT SHAPE OF EACH CORNER MAY VARY FROM DEPICTION.

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 7.000 BSC | | 0.276 BSC | |
| A1 | 3.500 BSC | | 0.138 BSC | |
| B | 7.000 BSC | | 0.276 BSC | |
| B1 | 3.500 BSC | | 0.138 BSC | |
| C | 1.400 | 1.600 | 0.055 | 0.063 |
| D | 0.300 | 0.450 | 0.012 | 0.018 |
| E | 1.350 | 1.450 | 0.053 | 0.057 |
| F | 0.300 | 0.400 | 0.012 | 0.016 |
| G | 0.800 BSC | | 0.031 BSC | |
| H | 0.050 | 0.150 | 0.002 | 0.006 |
| J | 0.090 | 0.200 | 0.004 | 0.008 |
| K | 0.500 | 0.700 | 0.020 | 0.028 |
| M | 12° REF | | 12° REF | |
| N | 0.090 | 0.160 | 0.004 | 0.006 |
| P | 0.400 BSC | | 0.016 BSC | |
| Q | 1° | 5° | 1° | 5° |
| R | 0.150 | 0.250 | 0.006 | 0.010 |
| S | 9.000 BSC | | 0.354 BSC | |
| S1 | 4.500 BSC | | 0.177 BSC | |
| V | 9.000 BSC | | 0.354 BSC | |
| V1 | 4.500 BSC | | 0.177 BSC | |
| W | 0.200 REF | | 0.008 REF | |
| X | 1.000 REF | | 0.039 REF | |

# 20
# F57J4 MASK SET DIFFERENCES

## 20.1 FUNCTIONAL DIFFERENCES

This section refers to MC145574 S/T–interfaces marked F57F4 and with a revision number BR15 = 03.

This mask set of the MC145574 has some functional differences from what is presented in this data book.

### 20.1.1 Differences in Section 6

In GCI TE master mode, the DCL = 2.048 MHz option is not available. (See Table 6–4.)

In GCI TE mode, B1 and B2 channels are enabled by default. NR5(3:2) bits allow the B channels to be set to idle 1s.

### 20.1.2 Differences in Section 10

OR6(3) is not available. In NT Terminal mode, the $D_{out}$ pin is always an open drain output.

### 20.1.3 Differences in Section 13.1.3.2

In NT Terminal mode, T_IN pin is only available when the device is activated. When the device is not activated, 2B+D data should be sent directly to the U–interface.

# A

# MC145574EVK ISDN S/T-INTERFACE TRANSCEIVER EVALUATION KIT

## A.1 INTRODUCTION

The MC145574EVK S/T–Interface Transceiver Evaluation Kit provides Motorola ISDN customers a convenient and efficient vehicle for evaluation of the MC145574 ISDN S/T–Interface Transceiver. The approach taken to demonstrate the MC145574 S/T–Interface Transceiver is to provide the user with a complete set of two S/T–Interfaces, either programmable for TE or NT modes. The MC145574EVK does not terminate any ISDN call control messages.

The kit provides the ability to interactively manipulate status registers in the MC145574 S/T–Interface Transceivers with the aid of an external terminal.

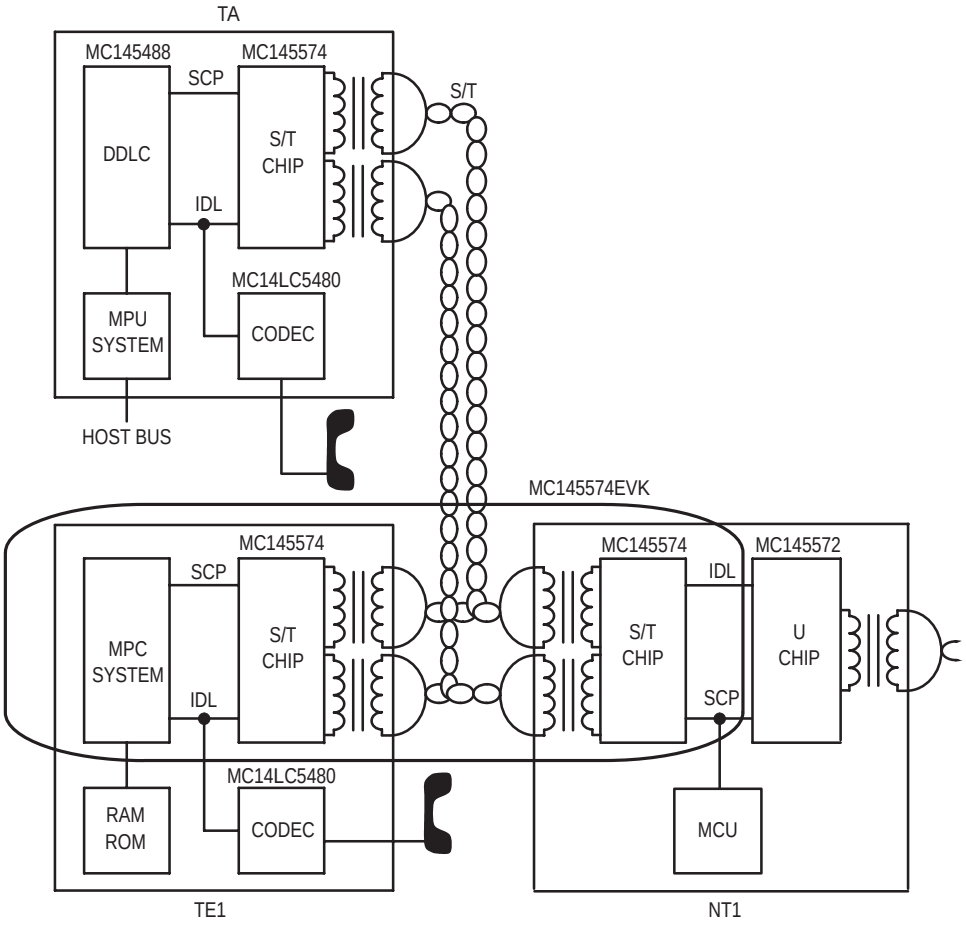



**Figure A–1. Motorola Silicon Applications and the MC145574EVK**

## A.2 FEATURES

### A.2.1 General

- Provides Standalone NT and TE on a Single Board
- On–Board 68HC11 Microcontroller With Resident Monitor Software
- Convenient Access to Key Signals
- NT and TE Software Development Platform

### A.2.2 Hardware

- Only + 5 Volt Power Supply
- Gated Data Clocks Provided for Bit Error Rate Testing
- Can Be Used as an S/T–Interface Terminal Development Tool
- EIA–232 (V.28) Serial Port for Terminal Interface

### A.2.3 Software

- Computer Operation
- Resident Firmware Monitor for User Control of Board
- Activation and Deactivation Menus
- MC68HC11 Assembly Language Source Code Available

## A.3 BLOCK DIAGRAM

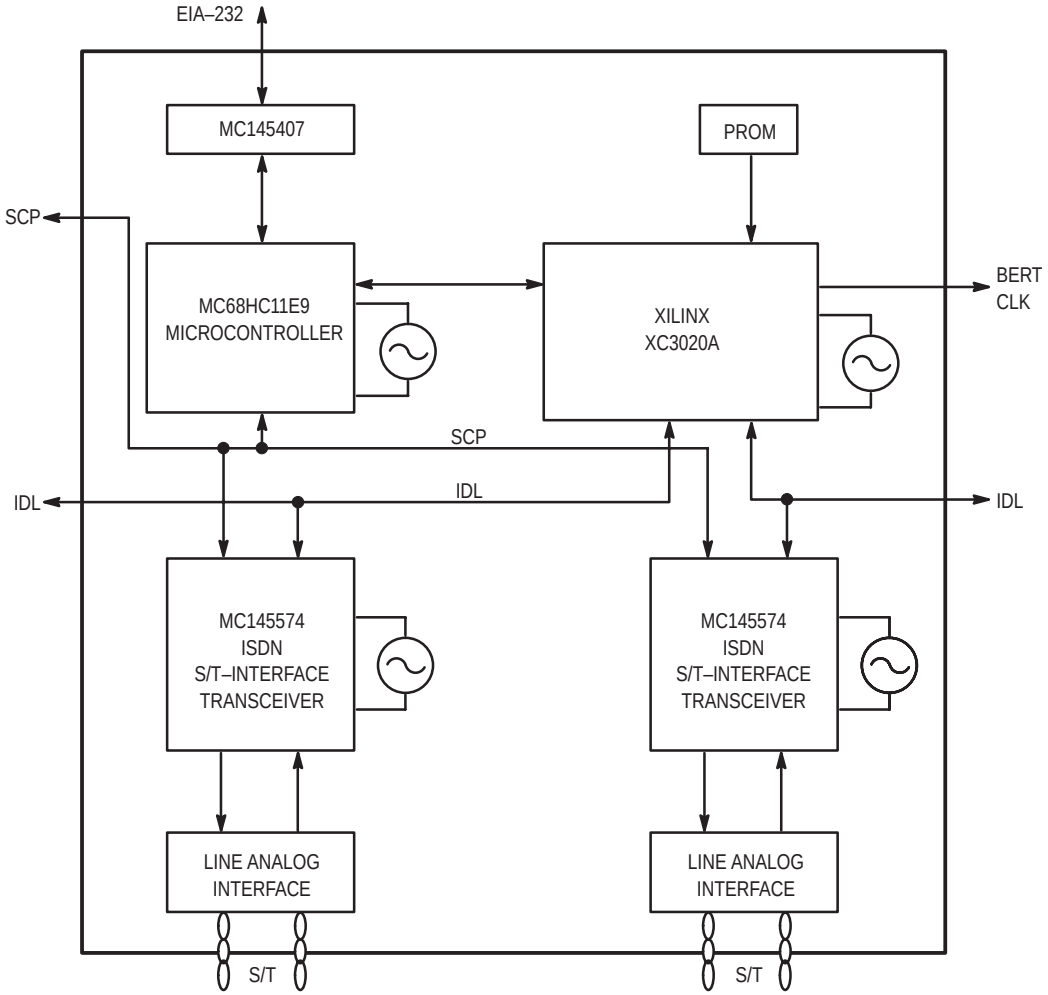



**Figure A–2. Block Diagram**

# B

# GLOSSARY OF TERMS AND ABBREVIATIONS

The list contains terms found in this and other Motorola publications concerned with Motorola Semiconductor products for Communications.

**A–Law** — A European companding/encoding law commonly used in PCM systems.

**A/B Signaling** — A special case of 8th–bit (LSB) signaling in a μ–law system that allows four logic states to be multiplexed with voice on PCM channels.

**A/D** (analog–to–digital) converter (ADC) — A converter that uniquely represents all analog input values within a specified total input range by a limited number of digital output codes, each of them exclusively representing a fractional part of the total analog input range.

**Aliasing Noise** — A distortion component that is created when frequencies present in a sampled signal are greater than one–half the sample rate.

**Answer Back** — A signal sent by receiving data–processing device in response to a request from a transmitting device, indicating that the receiver is ready to accept or has received data.

**Anti–Aliasing Filter** — A filter (normally low pass) that band limits an input signal *before* sampling to prevent aliasing noise.

**Asynchronous** — A mode of data transmission in which the time occurrence of the bits within each character or block of characters relates to a fixed time frame, but the start of each character or block of characters is not related to this fixed time frame.

**Attenuation** — A decrease in magnitude of a communication signal.

**Bandwidth** — The information–carrying frequencies between the limiting frequencies of a communication line or channel.

**Baseband** — The frequency band occupied by information–bearing signals before combining with a carrier in the modulation process.

**Baud** — A unit of signaling speed equal to the number of discrete signal conditions or events per second. This refers to the physical symbols/second used within a transmission channel.

**Bit Rate** — The speed at which data bits are transmitted over a communication path, usually expressed in bits per second. A 9600 bps terminal is a 2400 baud system with 4 bits/baud.

**Blocking** — A condition in a switching system in which no paths or circuits are available to establish a connection to the called party even though it is not busy, resulting in a busy tone to the calling party.

**BORS(C)HT** — Battery, Overvoltage, Ringing, Supervision, (Codec), Hybrid, Test; the functions performed by a subscriber line card in a telephone exchange.

**Broadband** — A transmission facility whose bandwidth is greater than that available on voice–grade facilities. (Also called wide band.)

**C Message** — A frequency weighting that evaluates the effects of noise based on its annoyance to the “typical” subscriber of standard telephone service or the effects of noise (background and impulse) on voice–grade data service.

**Carrier** — An analog signal of fixed amplitude and frequency that combines with an information–bearing signal by modulation to produce an output signal suitable for transmission.

**CCITT** — Consultative Committee for International Telephone and Telegraph; an international standards group of European International Telecommunications Union.

**CCSN** — Common Channel Signaling Network.

**Central Office (CO)** — A main telephone office, usually within a few miles of a subscriber, that houses switching gear; commonly capable of handling about 10,000 subscribers.

**Channel Bank** — Communication equipment commonly used for multiplexing voice–grade channels into a digital transmission signal (typically 24 channels in the U.S. and 30 channels in Europe).

**CIDCW** — Calling Identity Delivery on Call Waiting; a subscriber feature which allows for the display of the time, date, number, and possible other information about the caller to the called party while the called party is off–hook.

**CLASS** — Custom Local Area Signaling Service; a set of services, enhancements, provided to TELCO customers which may include CND, CNAM, Message Waiting, and other features.

**CLID** — Calling Line IDentification; a subscriber feature which allows for the display of the time, date, number, and possible other information about the caller to the called party.

**CNAM** — Calling Name Delivery; a subscriber feature which allows for the display of the time, date, number, and name of the caller to the called party.

**CND** — Calling Number Delivery; a subscriber feature which allows for the display of the time, date, number, and possible other information about the caller to the called party.

**CODEC** — COder–DECoder; the A/D and D/A function on a subscriber line card in a telephone exchange.

**COFIDEC** — COder–Filter–DECoder; the combination of a codec, the associated filtering, and voltage references required to code and decode voice in a subscriber line card.

**Common Mode Rejection** — The ability of a device having a balanced input to reject a voltage applied simultaneously to both differential–input terminals.

**Companding** — The process in which dynamic range compression of a signal is followed by expansion in accordance with a given transfer characteristic (companding law) which is usually logarithmic.

**Compander** — A combination of a compressor at one point in a communication path for reducing the amplitude range of signals, followed by an expander at another point for restoring the original amplitude range, usually to improve the signal–to–noise ratio.

**Conference Call** — A call between three or more stations, in which each station can carry on a conversation simultaneously.

**CPE** — Customer Premise Equipment; this could be a POTS phone, answering machine, fax machine, or any number of other devices connected to the PSTN.

**Crosspoint** — The operating contacts or other low–impedance–path connection over which conversations can be routed.

**Crosstalk** — The undesired transfer of energy from one signal path to another.

**CSN** — Circuit Switched Network.

**CTS** — Clear to send; a control signal between a modem and a controller used to initiate data transmission over a communication line.

**CVSD** — Continuous Variable Slope Delta (modulation); a simple technique to converting an analog signal (like voice) into a serial bit stream.

**D3** — D3 channel bank; a specific generation of AT&T 24–channel PCM terminal that multiplexes 24 voice channels into a 1.544 MHz digital bit stream. The specifications associated with D3 channel banks are the basis for all PCM device specifications.

**D/A** (digital–to–analog) converter (DAC) — A converter that represents a limited number of different digital input codes by a corresponding number of discrete analog output values.

**Data Compression** — A technique that provides for the transmission of fewer data bits than originally required without information loss. The receiving location expands the received data bits into the original bit sequence.

**dB** (decibel) — A power or voltage measurement unit, referred to another power or voltage. It is generally computed as:

10 x log (P1/P2) for power measurements, and

20 x log (V1/V2) for voltage measurements.

**dBm** — An indication of signal power. 1.0 mW across 600 Ω, or 0.775 volts rms, is defined as 0 dBm. Any other voltage level is converted to dBm by:

dBm = 20 x log (Vrms/0.775), or

dBm = [20 x log (Vrms)] + 2.22.

**dBmO** — Signal power measured at a point in a standard test tone level at the same point.

i.e., dBmO = dBm = dBr

where dBr is the relative transmission level, or level relative to the point in the system defined as the zero transmission level point.

**dBmOp** — Relative power expressed in dBmp. (See dBmO and dBmp.)

**dBmp** — Indicates dBm measurement made with a psophometric weighting filter.

**dBrn** — Relative signal level expressed in decibels above reference noise, where reference noise is 1 pW. Hence, 0 dBrn = 1 pW = – 90 dBm.

**dBrnC** — Indicates dBrn measurement made with a C–message weighting filter. (These units are most commonly used in the U.S., where psophometric weighting is rarely used.)

**dBrnc0** — Noise measured in dBrnc referenced to zero transmission level.

**Decoding** — A process in which one of a set of reconstructed analog samples is generated from the digital character signal representing a sample.

**Delay Distortion** — Distortion that occurs on communication lines due to the different propagation speeds of signals at different frequencies, measured in microseconds of delay relative to the delay at 1700 Hz. (This type of distortion does not affect voice communication, but can seriously impair data transmission.)

**Delta Modulation** — A simple digital coding technique that produces a serial bit stream corresponding to changes in analog input levels; usually utilized in devices employing continuously variable–slope delta (CVSD) modulation.

**Demodulator** — A functional section of a modem that converts received analog line signals to digital form.

**DN** — Directory Number.

**Digital Telephone** — A telephone terminal that digitizes a voice signal for transmission and decodes a received digital signal back to a voice signal. (It will usually multiplex 64 kbps voice and separate data inputs at multiples of 8 kbps.)

**Distortion** — The failure to reproduce an original signal's amplitude, phase, delay, etc. characteristics accurately.

**DPSK** — Differential Phase Shift Keying; a modulation technique for transmission where the frequency remains constant but phase changes will occur from 90°, 180°, and 290° to define the digital information.

**DTMF** — Dual Tone Multi–Frequency. It is the "tone dialing" system based on outputting two non–harmonic related frequencies simultaneously to identify the number dialed. Eight frequencies have been assigned to the four rows and four columns of a typical keypad.

**Duplex** — A mode of operation permitting the simultaneously two–way independent transmission of telegraph or data signals.

**Echo** — A signal that has been reflected or returned as a result of impedance mismatches, hybrid unbalance, or time delay. Depending upon the location of impedance irregularities and the propagation characteristics of a facility, echo may interfere with the speaker/listener or both.

**Echo Suppressor** — A device used to minimize the effect of echo by blocking the echo return currents; typically a voice–operated gate that allows communication one way at a time.

**Encoder** (PCM) — A device that performs repeated sampling, compression, and A/D conversion to change an analog signal to a serial stream of PCM samples representing the analog signal.

**Equalizer** — An electrical network in which phase delay or gain varies with frequency to compensate for an undesired amplitude or phase characteristic in a frequency–dependent transmission line.

**ET** — Exchange Termination (C.O. Switch).

**FDM** — Frequency–Division Multiplex; a process that permits the transmission of two or more signals over a common path by using a different frequency band for each signal.

**Four Wire Circuit** — The portion of a telephone, or central office, that operates on two pairs of wires. One pair is for the transmit path (generally from the microphone), and one pair is for the receive path (generally from the receiver).

**Frame** — A set of consecutive digit time slots in which the position of each digit slot can be identified by reference to a frame alignment. The frame alignment signal does not necessarily occur, in whole or in part, in each frame.

**Full Duplex** — A mode of operation permitting simultaneous transmission of information between two locations in both directions.

**Gain** — The change in signal amplitude (increase or decrease) after passing through an amplifier, or other circuit stage. Usually expressed in dB, an increase is a positive number, and a decrease is a negative number.

**Gain Tracking Error** — The variation of gain from a constant level (determined at 0 dBm input level) when measuring the dependence of gain on signal level by comparing the output signal to the input signal over a range of input signals.

**HDLC** — High–Level Data Link Control; a CCITT standard data communication line protocol.

**Half Duplex** — A transmission system that permits communication in one direction at a time. CB ratios, with “push–to–talk” switches, and voice–activated speakerphones, are half duplex.

**Handset** — A rigid assembly providing both telephone transmitter and receiver in a form convenient for holding simultaneously to mouth and ear.

**Hookswitch** — A switch that connects the telephone circuit to the subscriber loop. The name derives from old telephones where the switch was activated by lifting the receiver off and onto a hook on the side of the phone.

**Idle Channel Noise** (ICN) — The total signal energy measured at the output of a device or channel under test when the input of the device or channel is grounded (often a wide–band noise measurement using a C–message weighting filter to band–limit the output noise).

**Intermodulation** — The modulation of the components of a complex wave by each other (in a nonlinear system).

**Intermodulation Distortion** — An analog line impairment when two frequencies interact to create an erroneous frequency, in turn distorting the data signal representation.

**IRED** — Infrared. Used as a wireless link for remote control or to transfer data.

**ISDN** — Integrated Services Digital Network; a communication network intended to carry digitized voice and data multiplexed onto the public network.

**Jitter** — A type of analog communication line distortion caused by abrupt, spurious signal variation from a reference timing position, and capable of causing data transmission errors, particularly at high speeds. (The variation can be in amplitude, time, frequency, or phase.)

**Key System** — A miniature PABX that accepts 4 to 10 lines and can direct them to as many as 30 telsets.

**μ–law** — A companding law accepted as the North American standard for PCM based systems.

**LAN** — Local Area Network; a data–only communication network between data terminals using a standard interface to the network.

**Line** — The portion of a circuit external to an apparatus that consists of the conductors connecting the apparatus to the exchange or connecting two exchanges.

**Line Length Compensation** — Also referred to as loop length compensation, it involves changing the gain of the transmit and receive paths, within a telephone, to compensate for different signal levels at the end of different line lengths. A short line (close to the CO) will attenuate signals less, and therefore less gain is needed. Compensation circuits generally use the loop current as an indication of the line length.

**Longitudinal Balance** — The common–mode rejection of a telephone circuit.

**Loop** — The loop formed by the two subscriber wires (Tip and Ring) connected to the telephone at one end, and the central office (or PBX) at the other end. Generally it is a floating system, not referred to ground, or ac power.

**Loopback** — Directing signals back toward the source at some point along a communication path.

**Loop Current** — The dc current that flows through the subscriber loop. It is typically provided by the central office or PBX, and ranges from 20 to 120 mA.

**LT** — Line Termination (Line Card).

**MCU** — MicroComputer Unit (also MicroController Unit).

**MPU** — MicroProcessor Unit.

**Mu–Law** — A companding/encoding law commonly used in U.S. (same as μ–law).

**MUX** — Multiplex or multiplexer.

**Modem** — MOdulator–DEModulator; a unit that modulates and demodulates digital information from a terminal or computer port to an analog carrier signal for passage over an analog line.

**Multiframing** — When multiframing is enabled, 20 S/T frames are grouped together to provide maintenance subchannels between the TE and the NT. In the TE to NT direction, there is one subchannel called the Q channel. In the NT to TE direction, there are five subchannels called SC1 through SC5. Messages for the Q, SC1, and SC2 subchannels have been defined in CCITT I.430 and ANSI T1.605. Usage of the multiframing subchannels is not mandatory.

**Multiplex** — To simultaneously transmit two or more messages on a single channel.

**NT1** — Network Termination 1 (OSI Layer 1 Only).

**NT2** — Network Termination 2 (OSI Layers 2 and 3).

**Off–Hook** — The condition when the telephone is connected to the phone system, permitting loop current to flow. The central office detects the dc current as an indication that the phone is busy.

**On–Hook** — The condition when the telephone's dc path is open, and no dc loop current flows. The central office regards an on–hook phone as available for ringing.

**PABX** — Private Automatic Branch Exchange; a customer–owned, switchable telephone system providing internal and/or external station–to–station dialing.

**Pair** — The two associated conductors that form part of a communication channel.

**Pass–Band Filter** — A filter used in communication systems that allows only the frequencies within a communication channel to pass, and rejects all frequencies outside the channel.

**PBX** — Private Branch Exchange; a class of service in standard Bell System terminology that typically provides the same service as PABX.

**PCM** — Pulse Code Modulation; a method of transmitting data in which signals are sampled and converted to digital words that are then transmitted serially, typically as 8–bit words.

**Phase Jitter** — Abrupt, spurious variations in an analog line, generally caused by power and communication equipment along the line that shifts the signal phase relationship back and forth.

**PLL** — Phase–Locked Loop.

**PLL Frequency Synthesizer** — Phase–locked loop frequency synthesizer. A frequency synthesizer utilizing a closed loop, as opposed to DDS (direct digital synthesis) which is not a closed loop.

**POTS** — Plain Old Telephone Service.

**Propagation Delay** — The time interval between specified reference points on the input and output voltage waveforms.

**Psophometric Weighting** — A frequency weighting similar to C–Message weighting that is used as the standard for European telephone system testing.

**PSN** — Packet Switched Network.

**PSTN** — Public Switched Telephone Network.

**Pulse Dialer** — A device that generates pulse trains corresponding to digits or characters used in impulse or loop–disconnect dialing.

**Quantizing Noise** — Signal–correlated noise generally associated with the quantizing error introduced by A/D and D/A conversions in digital transmission systems.

**REN** — Ringer Equivalence Number; an indication of the impedance, or loading factor, of a telephone bell or ringer circuit. An REN of 1.0 equals about 8 kΩ. The Bell system typically permits a maximum of 5.0 REN (1.6 kΩ) on an individual subscriber line. A minimum REN of 0.2 (40 kΩ) is required by the Bell system.

**Repeater** — An amplifier and associated equipment used in a telephone circuit to process a signal and retransmit it.

**Repertory Dialer** — A dialer that stores a repertory of telephone numbers and dials any one of them automatically on request.

**Ring** — One of the two wires connecting the central office to a telephone. The name derives from the ring portion of the plugs used by operators (in older equipment) to make the connection. Ring is traditionally negative with respect to Tip.

**RTS** — Request To Send; an EIA–232 control signal between a modem and user's digital equipment that initiates the data transmission sequence on a communication line.

**Sampling Rate** — The frequency at which the amplitude of an analog signal is gated into a coder circuit. The Nyquist sampling theorem states that if a band–limited signal is sampled at regular intervals and at a rate equal to or greater than twice the highest frequency of interest, the sample contains all the information of the original signal. The frequency band of interest in telephony ranges from 300 to 3400 Hz, so a sampling rate of 8 kHz provides dc to 4000 Hz reproduction.

**SCU** — Subscriber Channel Unit; the circuitry at a telephone exchange associated with an individual subscriber line or channel.

**Sidetone** — The sound fed back to the receiver as a result of speaking into the microphone. It is a natural consequence of the 2–to–4 wire conversion system. Sidetone was recognized by Alexander Graham Bell as necessary for a person to be able to speak properly while using a handset.

**Signaling** — The transmission of control or status information between switching systems in the form of dedicated bits or channels of information inserted on trunks with voice data.

**Signal–to–Distortion Ratio** (S/D) — The ratio of the input signal level to the level of all components that are present when the input signal (usually a 1.020 kHz sinusoid) is eliminated from the output signal (e.g., by filtering).

**SLIC** — Subscriber Line Interface Circuit; a circuit that performs the 2–to–4 wire conversion, battery feed, line supervision, and common mode rejection at the central office (or PBX) end of the telephone line.

**SOG Package** — Small–Outline Gull–wing package; formerly SOIC with gull–wing leads. This package has leads which fold out from the body.

**SOJ Package** — Small–Outline J–lead package; formerly SOIC with J leads. This package has leads which are tucked under the body.

**Speech Network** — A circuit that provides 2–to–4 wire conversion, i.e., connects the microphone and receiver (or the transmit and receive paths) to the Tip and Ring phone lines. Additionally it provides sidetone control, and in many cases, the dc loop current interface.

**Subscriber Line** — The system consisting of the user's telephone, the interconnecting wires, and the central office equipment dedicated to that subscriber (also referred to as a loop).

**Switchhook** — A synonym for hookswitch.

**Syn (Sync)** — (1) A bit character used to synchronize a time frame in a time–division multiplexer. (2) A sequence used by a synchronous modem to perform bit synchronization or by a line controller for character synchronization.

**Synchronous Modem** — A modem that uses a derived clocking signal to perform bit synchronization with incoming data.

**T1 Carrier** — A PCM system operating at 1.544 MHz and carrying 24 individual voice–frequency channels.

**TA** — Terminal Adapter.

**Talkdown** — Missed signals in the presence of speech. Commonly used to describe the performance of a DTMF receiver when it fails to recognize a valid DTMF tone due to cancellation of that tone by speech.

**Talkoff** — False detections caused by speech. Commonly used to describe the performance of a DTMF receiver when speech, emulating DTMF, causes the receiver to believe it has detected a valid DTMF tone.

**Tandem Trunk** — See trunk.

**Telephone Exchange** — A switching center for interconnecting the lines that service a specific area.

**TE1** — Terminal Equipment 1 (ISDN Terminal).

**TE2** — Terminal Equipment 2 (Non–ISDN Terminal).

**TELETEX** — A text communication service between entirely electronic work stations that will gradually replace TELEX with the introduction of the digital network. (Not to be confused with teletext.)

**TELETEXT** — The name usually used for broadcast text (and graphics) for domestic television reception. (Not to be confused with teletex.)

**Time–Division Multiplex** — A process that permits the transmission of two or more signals over a common path by using a different time interval for each signal.

**Tin Cans and String** — A *crude* analog communications system commonly used to introduce voice communications to children.

**Tip** — One of the two wires connecting the central office to a telephone. The name derives from the tip of the plugs used by operators (in older equipment) to make the connection. Tip is traditionally positive with respect to ring.

**Tone Ringer** — The modern solid state equivalent of the old electromechanical bell. It provides the sound when the central office alerts the subscriber that someone is calling. Ringing voltage is typically 80–90 volts rms, 20 Hz.

**Trunk** — A telephone circuit or channel between two central offices or switching entities.

**TSAC** — Time Slot Assigner Circuit; a circuit that determines when a CODEC will put its 8 bits of data on a PCM bit stream.

**TSIC** — Time Slot Interchange Circuit; a device that switches digital highways in PCM based switching systems; a "digital" cross-point switch.

**Twist** — The amplitude ratio of a pair of DTMF tones. (Because of transmission and equipment variations, a pair of tones that originated equal in amplitude may arrive with a considerable difference in amplitude.)

**Two Wire Circuit** — Refers to the two wires connecting the central office to the subscriber's telephone. Commonly referred to as Tip and Ring, the two wires carry both transmit and receive signals in a differential manner.

**UDLT** — Universal Digital Loop Transceiver; a Motorola originated name for a voice/data transceiver circuit.

**VCO** — Voltage–controlled oscillator. Input is a voltage; output is a sinusoidal waveform.

**VCM** — Voltage–controlled multivibrator. Input is a voltage; output is a square wave.

**Voice Frequency** — A frequency within that part of the audio range that is used for the transmission of speech of commercial quality (i.e., 300–3400 Hz).

**Weighting Network** — A network whose loss varies with frequency in a predetermined manner.

# INDEX


## A

Activation, 3–1, 3–2, 6–14, 6–15, 8–3, 9–6, 9–8
    GCI, 6–14

Adaptive Timing, 13–1

ANSI T1.605, 1–2

## B

Byte Register, 5–3, 5–4, 9–1
    Initialization, 9–2
    Read, 5–3
    Write, 5–4

## C

CCITT I.430, 1–2

CLASS, 7–3

Class, 11–2

Clock, 4–9, 7–4, 14–1

Command Indicate Channel, 6–12

Configurations, 13–1
    NT, 13–1
    NT Fixed or Adaptive Timing, 13–1
    NT Terminal Mode, 13–2, 13–4
    TE Master Mode, 13–5
    TE Slave Mode, 13–5

Crystal, 5–7, 7–4, 14–1

## D

D Channel, 11–1, 15–1

Deactivate, 8–4

Deactivation, 3–3, 6–15
    GCI, 6–14

DGRANT, 7–2, 11–1

DREQUEST, 7–2, 11–1

## E

Echo Channel, 3–3, 9–7, 9–13

Error, 3–2, 8–3

ETSI ETS 300012, 1–2, 10–7

## F

Fixed Timing, 13–1

Frame Syncs, 4–4

## G

GCI, 6–1, 15–2
    Clock Frequency, 10–4
    D Channel Operation, 11–3
    DCL, 6–5
    Din, 6–5
    Direct, 6–6
    Dout, 6–5
    FSC, 6–5
    GCI Indirect Mode Enable, 10–4
    GCI Timeslot, S(2:0), 10–3
    Indirect, 6–4
    Modes, 6–1
    Multiframing, 12–3

## I

IDL2, 4–1, 4–2, 4–3, 4–9, 4–10, 9–8, 9–12
    Clock Speed (LSB), 9–8
    Clock Speed (MSB), 9–12
    Enable TCLK, 10–5

INFO State, 8–4, 9–11, 15–2

Initial State, 3–3

Interrupt, 8–6, 11–3
    Multiframe, 9–4

Interrupts, 15–1

## J

Jitter, 1–2

## L

Line Interface, 16–1

Long Frame, 4–8

Loopback, 8–7, 9–5

Loopbacks, 1–2

## M

M and N Parameters, 3–3

Master, 4–3, 7–2, 13–1
- GCI, 6–6

Monitor Channel, 6–7, 6–8, 6–11
- Commands, 6–10
- Messages, 6–8
- Operation, 6–8
- Response Messages, 6–10
- Status Indication Messages, 6–10

Multiframing, 1–2, 8–3, 8–5, 9–3, 9–7, 9–9, 12–1, 15–1
- Interrupts, 12–2

## N

Nibble Register, 5–1, 5–2, 8–1
- Initialization, 8–2
- Read, 5–1
- Write, 5–2

NT Terminal, 8–4, 10–6, 13–2

NT Terminal Mode, 8–5, 13–4

NT Terminal Modes, 1–2

NT1 Star, 2–3, 7–2, 9–12, 13–2

NT2, 13–6
- Applications, 4–8

## O

Overlay Register, 9–13, 10–1
- Enable, 10–7
- Initialization, 10–2

## P

Packages, 1–3

Passive Bus, 2–2, 2–3

Phase, 4–4, 4–5, 4–7

Pin Assignments, 19–1

Pin Descriptions, 7–1

Point–to–Point, 2–1

Power Settings, 17–1
- Absolute Minimum Power, 1–2, 8–2, 17–2
- Normal Power Operation, 17–1
- Sleep, 1–2, 17–2
- Transmit Power–Down, 1–2, 8–2, 17–1

Power–Down, 1–2, 8–2, 17–1

## R

Register Differences, 6–12

Register Maps, 8–1, 9–1, 9–2, 10–1

Reset, 7–4, 8–2

Revision, 9–13

## S

SCP, 5–1, 5–5, 5–7, 7–3, 7–5
- High–Impedance Digital Output Mode (SCP HIDOM), 5–7
- IRQ, 5–7
- Rx, 5–6
- SCPCLK, 5–6
- SCPEN, 5–7
- Slave, 5–7
- Tx, 5–6

Serial Control Port, 5–1

Slave, 4–2, 4–3, 4–11, 7–2, 10–5, 13–1
- Enable TCLK, 10–5
- GCI, 6–6
- TE Slave, 4–4

Sleep, 10–6, 17–2

## T

Terminal Mode, 6–7

Timeslot Assigner, 4–4
- Control Register, 10–4
- Rx B1 Channel Timeslot, 10–3
- Rx B2 Channel Timeslot, 10–3
- Rx D Channel Timeslot, 10–3
- Tx B1 Channel Timeslot, 10–2
- Tx B2 Channel Timeslot, 10–2
- Tx D Channel Timeslot, 10–2

Transformers, 16–3

Transmission States, 3–1

$\overline{\text{TSEN}}$, 4–2, 4–9, 4–11, 7–3, 10–5

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